ANNA UNIVERSITY, CHENNAI
UNIVERSITY DEPARTMENTS
M.E. APPLIED ELECTRONICS
REGULATIONS – 2015
CHOICE BASED CREDIT SYSTEM

PROGRAMME EDUCATIONAL OBJECTIVES:

1. Teach students to understand the principles involved in the latest hardware and software required for designing and critically analyzing electronic circuits relevant to industry and society
2. Blend theory and laboratory to make students appreciate the concepts in the working of electronic circuits
3. Mould students to be able to communicate effectively
4. Motivate students to take up socially relevant and challenging projects and propose innovative solutions to problems for the benefit of the society

PROGRAMME OUTCOMES:

Students will be able to:

a. Understand thoroughly the principles of electronic systems design
b. Gain expertise through hands on experience
c. Identify areas for the development of electronic hardware for the benefit of the society
d. Communicate general as well as technical information in an effective way
e. Handle technical and non-technical assignments individually or as a team member

MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMME OUTCOMES:

A broad relation between the programme objective and the outcomes is given in the following table:

PROGRAMME EDUCATIONAL OBJECTIVES	PROGRAMME OUTCOMES				
	a	b	c	d	e
1	✓	✓	✓	✓	✓
2	✓	✓	✓	✓	✓
3	✓	✓	✓	✓	✓
4	✓	✓	✓	✓	✓

			PO1	PO2	PO3	PO4	PO5
YEAR 1	SEM 1	Advanced Applied Mathematics	✓				
		Advanced Digital System Design	✓		✓	✓	✓
		Analog Integrated Circuit Design	✓		✓		✓
		Statistical Signal Processing	✓	✓	✓		✓
		Embedded Systems Design	✓		✓	✓	✓
		Digital CMOS VLSI Design	✓		✓		✓
		Embedded Systems Design Laboratory	✓	✓	✓		✓
	SEM 2	Digital Image Processing	✓	✓		✓	✓
		Digital Control Engineering	✓	✓			
		Elective I					
		Elective II					
		Elective III					
		Elective IV					
		Integrated Circuits Design Laboratory	✓	✓	✓		✓
		Technical Seminar and Report Writing					
YEAR 2	SEM 1	Elective V					
		Elective VI					
		Elective VII					
		Project Work Phase I	✓	✓	✓	✓	✓
	SEM 2	Project Work Phase II	✓	✓	✓	✓	✓

ANNA UNIVERSITY, CHENNAI
UNIVERSITY DEPARTMENTS
M.E. APPLIED ELECTRONICS - (FT & PT)
REGULATIONS – 2015
CHOICE BASED CREDIT SYSTEM
CURRICULA AND SYLLABI

SEMESTER - I

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	MA 7152	Advanced Applied Mathematics	FC	4	4	0	0	4
2.	AP 7151	Advanced Digital System Design	PC	3	3	0	0	3
3.	AP 7152	Analog Integrated Circuit Design	PC	3	3	0	0	3
4.	AP 7154	Statistical Signal Processing	PC	3	3	0	0	3
5.	AP 7153	Embedded Systems Design	PC	3	3	0	0	3
6.	VL 7152	Digital CMOS VLSI Design	PC	3	3	0	0	3
PRACTICALS								
7.	AP 7111	Embedded Systems Design Laboratory	PC	2	0	0	4	2
			TOTAL	**21**	**19**	**0**	**4**	**21**

II SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	AP 7252	Digital Image Processing	PC	3	3	0	0	3
2.	AP 7251	Digital Control Engineering	PC	3	3	0	0	3
3.		Elective I	PE	3	3	0	0	3
4.		Elective II	PE	3	3	0	0	3
5.		Elective III	PE	3	3	0	0	3
6.		Elective IV	PE	3	3	0	0	3
PRACTICALS								
7.	AP 7211	Integrated Circuits Design Laboratory	PC	4	0	0	4	2
8.	AP 7212	Technical Seminar and Report Writing	EEC	2	0	0	2	1
			TOTAL	**24**	**18**	**0**	**6**	**21**

III SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.		Elective V	PE	3	3	0	0	3
2.		Elective VI	PE	3	3	0	0	3
3.		Elective VII	PE	3	3	0	0	3
PRACTICALS								
4.	AP 7311	Project Work Phase I	EEC	12	0	0	12	6
			TOTAL	**21**	**9**	**0**	**12**	**15**

IV SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
PRACTICALS								
1.	AP 7411	Project Work Phase II	EEC	24	0	0	24	12
			TOTAL	**24**	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS:69

ANNA UNIVERSITY, CHENNAI

UNIVERSITY DEPARTMENTS

M.E. APPLIED ELECTRONICS - (FT & PT)

REGULATIONS – 2015

CHOICE BASED CREDIT SYSTEM

CURRICULUM I TO VI SEMESTERS (PART TIME)

I SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	MA 7152	Advanced Applied Mathematics	FC	4	4	0	0	4
2.	AP 7151	Advanced Digital System Design	PC	3	3	0	0	3
3.	AP 7154	Statistical Signal Processing	PC	3	3	0	0	3
			TOTAL	**10**	**10**	**0**	**0**	**10**

II SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	AP 7252	Digital Image Processing	PC	3	3	0	0	3
2.	AP 7251	Digital Control Engineering	PC	3	3	0	0	3
3.		Elective I	PE	3	3	0	0	3
			TOTAL	**9**	**9**	**0**	**0**	**9**

III SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	AP 7152	Analog Integrated Circuit Design	PC	3	3	0	0	3
2.	AP 7153	Embedded Systems Design	PC	3	3	0	0	3
3.	VL 7152	Digital CMOS VLSI Design	PC	3	3	0	0	3
PRACTICALS								
4.	AP 7111	Embedded Systems Design Laboratory	PC	4	0	0	4	2
			TOTAL	**13**	**9**	**0**	**4**	**11**

IV SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.		Elective II	PE	3	3	0	0	3
2.		Elective III	PE	3	3	0	0	3
3.		Elective IV	PE	3	3	0	0	3
PRACTICALS								
4.	AP 7211	Integrated Circuits Design Laboratory	PC	4	0	0	4	2
5.	AP 7212	Technical Seminar and Report Writing	EEC	2	0	0	2	1
			TOTAL	**15**	**9**	**0**	**6**	**12**

V SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.		Elective V	PE	3	3	0	0	3
2.		Elective VI	PE	3	3	0	0	3
3.		Elective VII	PE	3	3	0	0	3
PRACTICALS								
4.	AP 7311	Project Work Phase I	EEC	12	0	0	12	6
			TOTAL	**21**	**9**	**0**	**12**	**15**

VI SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
PRACTICALS								
1.	AP 7411	Project Work Phase II	EEC	24	0	0	24	12
			TOTAL	**24**	0	0	24	12

TOTAL NO. OF CREDITS:69

FOUNDATION COURSES (FC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.		Advanced Applied Mathematics	FC	4	4	0	0	4

PROFESSIONAL CORE (PC)

SL. NO	Course Code	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.		Advanced Digital System Design	PC	3	3	0	0	3
2.		Analog Integrated Circuit Design	PC	3	3	0	0	3
3.		Embedded Systems Design	PC	3	3	0	0	3
4.		Statistical Signal Processing	PC	3	3	0	0	3
5.		Digital CMOS VLSI Design	PC	3	3	0	0	3
6.		Embedded Systems Design Laboratory	PC	4	0	0	4	2
7.		Digital Control Engineering	PC	3	3	0	0	3
8.		Digital Image Processing	PC	3	3	0	0	3
9.		Integrated Circuits Design Laboratory	PC	4	0	0	4	2

PROFESSIONAL ELECTIVES (PE)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	AP 7002	Power Electronics	PE	3	3	0	0	3
2.	AP 7003	Synthesis and Optimization of Digital Circuits	PE	3	3	0	0	3
3.	AP 7071	Advanced Microprocessors and Microcontrollers	PE	3	3	0	0	3
4.	AP7072	Artificial Intelligence and Optimization Techniques	PE	3	3	0	0	3
5.	AP 7073	Design and Analysis of Computer Algorithms	PE	3	3	0	0	3
6.	AP 7076	Hardware and Software Co Design	PE	3	3	0	0	3
7.	AP 7077	Introduction to MEMS System Design	PE	3	3	0	0	3
8.	AP 7078	Nonlinear Signal Processing	PE	3	3	0	0	3

9.	AP 7080	Selected Topics in ASIC Design	PE	3	3	0	0	3
10.	AP 7081	Selected Topics in IC Design	PE	3	3	0	0	3
11.	AP 7082	Signal Integrity For High Speed Design	PE	3	3	0	0	3
12.	AP 7083	Wireless Sensor Networks	PE	3	3	0	0	3
13.	VL 7252	Low Power VLSI Design	PE	3	3	0	0	3
14.	VL 7071	Solid State Device Modeling and Simulation	PE	3	3	0	0	3
15.	VL 7072	Testing of VLSI Circuits	PE	3	3	0	0	3
16.	VL 7073	VLSI Signal Processing	PE	3	3	0	0	3
17.	VL 7151	CAD For VLSI Circuits	PE	3	3	0	0	3
18.	VL 7251	Data Converters	PE	3	3	0	0	3
19.	AP 7001	Advanced Computer Architecture Design	PE	3	3	0	0	3
20.	AP 7075	Electromagnetic Interference and Compatibility in System Design	PE	3	3	0	0	3
21.	AP 7079	RF System Design	PE	3	3	0	0	3
22.	AP 7074	DSP Integrated Circuits	PE	3	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.		Technical Seminar and Report Writing	EEC	2	0	0	2	1
2.		Project Work Phase I	EEC	12	0	0	12	6
3.		Project Work Phase II	EEC	24	0	0	24	12

MA 7152 ADVANCED APPLIED MATHEMATICS L T P C
4 0 0 4

OBJECTIVES:

- To encourage students to develop a working knowledge of the central ideas of linear algebra.
- To study and understand the concepts of probability and random variable of the various functions.
- understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete-time Markov chains.
- To formulate and construct a mathematical model for a linear programming problem in real life situation.
- Introduce the Fourier Transform as an extension of Fourier techniques on periodic functions and to solve partial differential equations.

UNIT I LINEAR ALGEBRA 9+3

Vector spaces – norms – Inner Products – Eigenvalues using QR transformations – QR factorization - generalized eigenvectors – Canonical forms – singular value decomposition and applications - pseudo inverse – least square approximations --Toeplitz matrices and some applications.

UNIT II ONE DIMENSIONAL RANDOM VARIABLES 9+3

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT III RANDOM PROCESSES 9+3

Classification – Auto correlation - Cross correlation - Stationary random process – Markov process –- Markov chain - Poisson process – Gaussian process.

UNIT IV LINEAR PROGRAMMING 9+3

Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

UNIT V FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS 9+3

Fourier transforms: Definitions, properties-Transform of elementary functions, Dirac Delta functions – Convolution theorem – Parseval's identity – Solutions to partial differential equations: Heat equations, Wave equations, Laplace and Poison's equations.

TOTAL: 45+15:60 PERIODS

OUTCOMES:

On successful completion of this course, all students will have developed knowledge and understanding in the fields of linear algebra, probability, stochastic process, linear programming problem and Fourier transform.

TEXT BOOKS:

1. Bronson, R.Matrix Operation, Schaum's outline series, McGrawHill, Newyork 1989.
2. Oliver C. Ibe, "Fundamentals of Applied Probability and Random Processes, Academic Press, (An imprint of Elsevier), 2010.
3. Taha H.A. "Operations Research : An introduction" Ninth Edition, Pearson Education, Asia, New Delhi 2012.
4. Sankara Rao, K. "Introduction to partial differential equations" Prentice Hall of India, pvt, Ltd, New Delhi, 1997.

REFERENCES:
1. Andrews,L.C. and Philips.R.L. "Mathematical Techniques for engineering and scientists", Printice Hall of India,2006.
2. O'Neil P.V. "Advanced Engineering Mathematics", (Thomson Asia pvt ltd, Singapore) 2007, cengage learning India private limited.

AP 7151	**ADVANCED DIGITAL SYSTEM DESIGN**	**L T P C**
		3 0 0 3

OBJECTIVES:
- To introduce methods to analyze and design synchronous and asynchronous sequential circuits
- To introduce the architectures of programmable devices
- To introduce design and implementation of digital circuits using programming tools

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

TOTAL : 45 PERIODS

OUTCOMES:
- Analyze and design sequential digital circuits
- Identify the requirements and specifications of the system required for a given application
- Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:
1 Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004
2 Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001
3 Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002
4 Parag K.Lala "Digital system Design using PLD" B S Publications,2003
5 M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.
6 M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
7 S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

AP 7152 ANALOG INTEGRATED CIRCUIT DESIGN **L T P C**
3 0 0 3

OBJECTIVES:

- Analog circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology. The most important building blocks of all CMOS analog ICs will be the topic of study in this course.
- The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.
- The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.

UNIT I SINGLE STAGE AMPLIFIERS 12

Basic MOS physics and equivalent circuits and models, CS,, CG and Source Follower cascocde and folded cascade configurations, differential amplifiers and current mirror configurations.

UNIT II HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS 9

Current mirrors, cascode stages for current mirrors, current mirror loads for differential pairs. Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III FEEDBACK AND OPERATIONAL AMPLIFIERS 9

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION 9

General considerations, Multipole systems,Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

UNIT V BANDGAP REFERENCES 6

Supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

TOTAL: 45 PERIODS

OUTCOMES:
At the end of the course, the student should be able to:

- Determine the device dimensions of MOSFETs.
- Discuss the most important building blocks of all CMOS analog ICs.
- Analyze the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design.
- Design single and multistage voltage, current and differential amplifiers.

REFERENCES:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001
2. Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006.
3. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & sons,Inc., 2003.
4. Phillip E.Allen, DouglasR.Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2002
5. Recorded lecture available at http://www.ee.iitm.ac.in/~ani/ee5390/index.html
   Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010 3rd Edition

AP 7154	STATISTICAL SIGNAL PROCESSING	L T P C
		3 0 0 3

OBJECTIVES:

- To introduce the basics of random signal processing
- To learn the concept of estimation and prediction theory
- To know about adaptive filtering and it's applications
- To understand the processing of speech signals

UNIT I INTRODUCTION TO RANDOM SIGNAL PROCESSING 9

Discrete Random Processes- Ensemble Averages, Stationary processes, Bias and Estimation, Autocovariance, Autocorrelation, Parseval's theorem, Wiener-Khintchine relation, White noise, Power Spectral Density, Spectral factorization, Filtering Random Processes, Special types of Random Processes – ARMA, AR, MA – Yule-Walker equations.

UNIT II SPECTRAL ESTIMATION 9

Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric method, AR (p) spectral estimation and detection of Harmonic signals, MUSIC algorithm.

UNIT III LINEAR ESTIMATION AND PREDICTION 9

Linear Prediction of Signals-Forward and Backward Predictions, Solution to Prony's normal equation, Levinson Durbin Algorithm, Lattice filter realization of prediction error filters. Linear Minimum Mean-Square Error (LMMSE) Filtering: Wiener Hopf Equation, FIR Wiener filter, Noise Cancellation, Causal IIR Wiener filter, Noncausal IIR Wiener filter, Discrete Kalman filter

UNIT IV ADAPTIVE FILTERS 9

FIR adaptive filters – adaptive filter based on steepest descent method- Widrow-Hopf LMS algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo cancellation, Adaptive noise cancellation, RLS adaptive algorithm.

UNIT V APPLICATION OVERVIEW-SPEECH PROCESSING 9

Speech Fundamentals: Articulatory Phonetics – Production and Classification of Speech Sounds; Acoustic Phonetics – acoustics of speech production; Short-term Fourier transform (STFT): overview of Fourier representation, non-stationary signals, development of STFT, transform and filter-bank views of STFT; Short time Homomorphic Filtering of Speech; Linear Prediction (LP) analysis: Basis and development, Levinson-Durbin's method, normalized error, LPC spectrum.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Estimate the spectra from finite duration signal
- Analyze non-parametric methods and parametric methods for spectral estimation
- Design different MMSE filters
- Obtain models for prediction and Estimation
- Design adaptive filters for different applications
- Analyze different speech signal processing techniques
- Represent acoustic signal in Short-term Fourier Transform

REFERENCES:

1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc, Singapore, 2002.
2. Lawrence Rabiner and Biing-Hwang Juang, "Fundamentals of Speech Recognition", Pearson Education, 2003.
3. Dimitris G. Manolakis and Vinay K .Ingle ,"Applied Digital Signal Processing", Cambridge University Press, 2011.
4. L.R. Rabiner and R.W. Schafer, "Introduction to Digital Speech Processing" (Foundations and Trends in Signal Processing), Now Publishers Inc.,USA, 2007.

AP 7153 EMBEDDED SYSTEMS DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To expose the students to the fundamentals of embedded system design.
- To enable the students to understand and use embedded computing platform.
- To introduce networking principles in embedded devices.
- To introduce RTOS in embedded devices.

UNIT I EMBEDDED PROCESSORS 9

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM 9

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture

UNIT III NETWORKS 9

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS 9

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES 9

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer-Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL : 45 PERIODS

OUTCOMES:

- Able to select and design suitable embedded systems for real world applications.

REFERENCES:

1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers.
2. Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia.
3. C. M. Krishna and K. G. Shin, “Real-Time Systems” , McGraw-Hill, 1997
4. Frank Vahid and Tony Givargis, “Embedded System Design: A Unified Hardware/Software Introduction” , John Wiley & Sons.

VL7152 DIGITAL CMOS VLSI DESIGN L T P C
3 0 0 3

OBJECTIVES:

- This course deals comprehensively with all aspects of transitor level design of all the digital building blocks common to all CMOS microproceesors, DPSs, network processors, digital backend of all wireless systems etc.
- The focus will on the transistor level design and will address all important issues related to size, speed and power consumption. The units are classified according to the important building and will introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore’s constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Nonbistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V INTERCONNECT AND CLOCKING STRATEGIES 6

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.
- Discuss design methodology of arithmetic building block
- Analyze tradeoffs of the various circuit choices for each of the building block.

REFERENCES:

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective". Second Edition, Feb 2003, Prentice Hall of India.
2. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". Second Edition, 1993 Addision Wesley,
3. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
   Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley
   IEEE Press 2010 3rd Edition

AP 7111 EMBEDDED SYSTEMS DESIGN LABORATORY L T P C
0 0 4 2

OBJECTIVES:

- To give a hands on programming experience using microcontrollers.
- To induce a programming skill in embedded system design using KEIL or RIDE software.

1. Board development using 8051 microcontroller
2. Assembly and High level language programs for 8051 - ports – timers -Seven Segment display – I^2C – LCD interface
3. RTOS – Simple task creation, Round Robin Scheduling, Preemptive scheduling, Semaphores, Mailboxes.
4. Assembly and High level language programs for R8C - ports – timers -Seven Segment display – I^2C – LCD interface – Stepper Motor control
5. Assembly and High level language programs for MSP 430 - ports – timers - Seven Segment display – I^2C – LCD interface – Stepper Motor control

TOTAL : 60 PERIODS

OUTCOMES:

- Ability to gain the skill of effective design of embedded systems using different microcontrollers.

AP 7252 DIGITAL IMAGE PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To provide an introduction to basic concepts and methodologies for digital image processing.
- To develop engineering skills and intuitive understanding of the most important concepts, techniques and algorithms for digital image processing.
- To understand the general processes of image acquisition, storage, enhancement, segmentation, representation and description.
- To implement filtering and enhancement algorithms for monochrome as well as color images.
- To appreciate the challenges and understand the principles and applications of visual pattern recognition.

UNIT I DIGITAL IMAGE FUNDAMENTALS 9

Elements of digital image processing systems, Digital Camera working principles, Elements of visual perception, brightness, contrast, hue, saturation, Mach Band effect, Image sampling, Quantization, Dither, Two dimensional mathematical preliminaries.

UNIT II IMAGE TRANSFORMS 9

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III IMAGE ENHANCEMENT AND RESTORATION 9

Spatial domain filtering, intensity transformations, contrast stretching, histogram equalization, smoothing filters, sharpening filters, noise distributions, mean filters, order statistics filters. Image restoration - degradation model, Unconstrained and Constrained restoration, Inverse filtering-removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations-spatial transformations, Gray-Level interpolation.

UNIT IV IMAGE SEGMENTATION AND MORPHOLOGY 9

Image segmentation - Edge detection, Edge linking and boundary detection, Region growing, Region splitting and Merging, Image Recognition - Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation, Morphological Image Processing - Basics, SE, Erosion, Dilation, Opening, Closing, Hit-or-Miss Transform, Boundary Detection, Hole filling, Connected components, convex hull, thinning, thickening, skeletons, pruning, Geodesic Dilation, Erosion, Reconstruction by dilation and erosion.

UNIT V IMAGE COMPRESSION 9

Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding, Transform coding, JPEG, MPEG.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Develop an overview of the field of image processing.
- Outine and implement the fundamental algorithms
- Gain experience in applying image processing algorithms to real problems

REFERENCES:

1. Rafael C. Gonzalez, Richard E. Woods, “ Digital Image Processing”, Pearson Education, Inc., Second Edition, 2004
2. Anil K. Jain, “Fundamentals of Digital Image Processing”, Prentice Hall of India, 2002.
3. Rafael C. Gonzalez, Richard E. Woods, Steven Eddins,” Digital Image Processing using MATLAB”, Pearson Education, Inc., 2004.

4. William K. Pratt, " Digital Image Processing", John Wiley, New York, 2002.
5. S. Sridhar, " Digital Image Processing", Oxford University Press.
6. Milan Sonka et al, "Image Processing, Analysis and Machine Vision", Brookes/Cole, Vikas Publishing House, 2nd edition, 1999;
7. Sid Ahmed, M.A., " Image Processing Theory, Algorithms and Architectures", McGrawHill, 1995.

AP 7251 DIGITAL CONTROL ENGINEERING L T P C
3 0 0 3

OBJECTIVES:

- Students should acquire a fundamental understanding of digital control systems and design.
- To teach the fundamental concepts of Digital Control systems and mathematical modeling of the system
- To study the concept of time response and frequency response of the discrete time system
- To teach the basics of stability analysis of the digital system

UNIT I PRINCIPLES OF CONTROLLERS 9

Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9

Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM 9

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9

Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

TOTAL : 45 PERIODS

OUTCOMES:

- Acquire working knowledge of discrete system science-related mathematics.
- Design a discrete system, component or process to meet desired needs.
- Identify, formulate and solve discrete control engineering problems.
- Use the techniques, tools and skills related to discrete signals, computer science and modern discrete control engineering in modern engineering practice
- Communicate system related concepts effectively

REFERENCES

1. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.
2. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995.
3. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.

AP 7211 INTEGRATED CIRCUITS DESIGN LABORATORY L T P C
0 0 4 2

OBJECTIVES:

- To introduce the programming concepts using Verilog or VHDL
- To introduce the concepts of system design using FPGA

1. Design Entry Using VHDL or Verilog, examples for circuit descriptions using HDL languages sequential and concurrent statements.
2. Structural and behavioral descriptions, principles of operation and limitation of HDL simulators. Examples of sequential and combinational logic design and simulation. Test vector generation.
3. CPLD – Board development. I/O interfacing, Analog interfacing, Real time application development.
4. FPGA- Board development. I/O interfacing, Analog interfacing, Real time application development.
5. System development using either PSPICE or FPGAs

OUTCOMES:

- Ability to develop FPGA based system design.

AP 7002 POWER ELECTRONICS L T P C
3 0 0 3

OBJECTIVES:

- To introduce electronic circuits for power control in industry and home applications
- To design electronic circuits for efficient power control.

UNIT I CONVERTERS IN EQUILIBRIUM 9

Principles of Steady State Converter Analysis – Boost and Buck Converter Examples Steady-State Equivalent Circuit Modeling, Losses, and Efficiency – Equivalent circuit model – complete circuit model - - Switch Realization- Switching loss - Converter Circuits – Circuit manipulation – Transformer isolation – Converter evaluation and design

UNIT II CONVERTER DYNAMICS AND CONTROL 9

The Basic AC Modeling Approach - Averaging the Inductor and capacitor Waveforms - A Nonideal Flyback Converter - State-Space Averaging - Circuit Averaging and Averaged Switch Modeling - The Canonical Circuit Model - Converter Transfer Functions - Analysis of Converter Transfer Functions - Graphical Construction of Impedances and Transfer Functions - Controller Design - Input Filter Design- Current Programmed Control

UNIT III MAGNETICS 9

Basic Magnetics Theory - Transformer Modeling - Loss Mechanisms in Magnetic Devices - Eddy Currents in Winding Conductors - Inductor Design - Filter Inductor Design Constraints - A Step-by-Step Procedure - Transformer Design - A Step-by-Step Transformer Design Procedure

UNIT IV MODERN RECTIFIERS AND POWER SYSTEM HARMONICS 9

Power Phasors in Sinusoidal Systems - Harmonic Currents in Three-Phase Systems - AC Line Current Harmonic Standards - **Line-Commutated Rectifiers -** The Single-Phase Full-Wave Rectifier - The Three-Phase Bridge Rectifier - Phase Control - **Pulse-Width Modulated Rectifiers -** Realization of a Near-Ideal Rectifier - Control of the Current Waveform - Ideal Three-Phase Rectifiers

UNIT V RESONANT CONVERTERS 9

Resonant Conversion - Sinusoidal Analysis of Resonant Converters – Examples - Soft Switching - Soft-Switching Mechanisms of Semiconductor Devices - The Zero-Current-Switching Quasi-Resonant Switch Cell - Resonant Switch Topologies - Soft Switching in PWM Converters.

TOTAL : 45 PERIODS

OUTCOMES:

- Ability to analyze and design electronic circuits for efficient power control.

REFERENCES:

1. Robert W. Erickson, Dragan Maksimovic," Fundamentals of Power Electronics", Kluwer Academic Publishers, Second Edition, New York, Boston, Dordrecht, London, Moscow.
2. Muhammad H Rashid, " Power Electronics – Circuits, Devices and Applications", Third Edition, Prentice Hall of India, 2004.
3. M.D. Singh, K.B.Khanchandani, " Power Electronics", Tata McGraw Hill, 1998.
4. Ned Mohan, Tore M Undeland, William P. Robbins, Power Electronics, Converters, Applications and Design", John Wiley & Sons, 1994.

AP 7003 SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- Deals with the basics of synthesis optimization, scheduling algorithms and resource allocation algorithms for CAD synthesis.
- To teach the logic level synthesis for combinational as well as sequential circuits and technology mapping.

UNIT I CIRCUITS AND HARDWARE MODELING 9

Design of Microelectronic Circuits - Computer Aided Synthesis and optimization-Combinatorial optimization-Boolean Algebra and Application-Hardware Modeling Languages –Compilation and Behavioral optimization.

UNIT II ARCHITECTURAL LEVEL SYNTHESIS AND OPTIMIZATION 9

The Fundamental Architectural synthesis Problems-Area and performance Estimation-Control unit synthesis-synthesis of pipelined circuits.

UNIT III SCHEDULING ALGORITHMS AND RESOURCE SHARING 9

Unconstrained Scheduling-ASAP Algorithm-ALAP Scheduling Algorithm- Scheduling with Resource Constraints- Scheduling pipelined circuits-Sharing and binding for Dominated circuits-Area Binding-Concurrent Binding –Module selection problems-Structural testability.

UNIT IV LOGIC-LEVEL SYNTHESIS AND OPTIMIZATION 9

Logic optimization Principles-Algorithms and logic Minimization –Encoding problems- Multiple-level optimization of logic networks-Algebraic and Boolean model-Algorithm for delay Evaluation-Rule based logic optimization.

UNIT V SEQUENTIAL LOGIC OPTIMIZATION 9

Sequential circuit -State Encoding-Minimization methods-Retiming- Finite state machine-testability for synchronous circuits-Algorithm for library binding- Look-Up table - FPGA- Rule-based library binding.

TOTAL : 45 PERIODS

OUTCOMES:

- Capability to design , synthesize and optimize combinational as well as sequential circuits.
- Ability to modify the digital designs for optimal performance using different scheduling and resource allocation algorithms.

REFERENCES:

1. Giovanni De Micheli, “Synthesis and optimization of Digital Circuits”, Tata McGraw-Hill, 2003.
2. John Paul Shen, Mikko H. Lipasti, “Modern processor Design”, Tata McGraw Hill, 2003

AP 7071 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS L T P C
3 0 0 3

OBJECTIVES:

- To expose the students to the fundamentals of microprocessor architecture.
- To introduce the advanced features in microprocessors and microcontrollers.
- To enable the students to understand various microcontroller architectures.

UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS 9

Instruction set addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.

UNIT V PIC MICROCONTROLLER 9

CPU Architecture – Instruction set – interrupts- Timers- I^2C Interfacing –UART- A/D Converter – PWM and introduction to C-Compilers.

TOTAL: 45 PERIODS

OUTCOME:

- The student will be able to work with suitable microprocessor / microcontroller for a specific real world application.

REFERENCES:

1. Daniel Tabak , ‘’ Advanced Microprocessors” McGraw Hill.Inc., 1995
2. James L. Antonakos , “ The Pentium Microprocessor ‘’ Pearson Education , 1997.
3. Steve Furber , ‘’ ARM System –On –Chip architecture “Addision Wesley , 2000.
4. Gene .H.Miller .” Micro Computer Engineering ,” Pearson Education , 2003.
5. John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.
6. James L.Antonakos ,” An Introduction to the Intel family of Microprocessors ‘’ Pearson Education 1999.
7. Barry.B.Breg,” The Intel Microprocessors Architecture , Programming and Interfacing “ , PHI,2002.
8. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001. Readings: Web links www.ocw.nit.edu www.arm.com

AP 7072 ARTIFICIAL INTELLIGENCE AND OPTIMIZATION TECHNIQUES L T P C
3 0 0 3

OBJECTIVES:

- To introduce the techniques of computational methods inspired by nature, such as neural networks, genetic algorithms and other evolutionary computation systems, ant swarm optimization, artificial immune systems, cellular automata, and multi-agent systems.
- To present main rules underlying in these techniques.
- To present selected case-studies.
- To adopt these techniques in solving problems in the real world.

UNIT I NEURAL NETWORKS 9

Neural Networks: Back Propagation Network, generalized delta rule, Radial Basis Function Network, interpolation and approximation RBFNS, comparison between RBFN and BPN, Support Vector Machines : Optimal hyperplane for linearly separable patterns, optimal hyperplane for non-linearly separable patterns, Inverse Modeling.

UNIT II FUZZY LOGIC SYSTEMS 9

Fuzzy Logic System: Basic of fuzzy logic theory , crisp and fuzzy sets, Basic set operation like union , interaction , complement , T-norm , T-conorm , composition of fuzzy relations, fuzzy if-then rules , fuzzy reasoning, Neuro-Fuzzy Modeling: Adaptive Neuro-Fuzzy Inference System (ANFIS) , ANFIS architecture , Hybrid Learning Algorithm.

UNIT III EVOLUTIONARY COMPUTATION AND GENETIC ALGORITHMS 9

Evolutionary Computation (EC) – Features of EC – Classification of EC – Advantages – Applications. Genetic Algorithms: Introduction – Biological Background – Operators in GA-GA Algorithm – Classification of GA – Applications

UNIT IV ANT COLONY OPTIMIZATION 9

Ant Colony Optimization: Introduction – From real to artificial ants- Theoretical considerations – Convergence proofs – ACO Algorithm – ACO and model based search – Application principles of ACO.

UNIT V PARTICLE SWARM OPTIMIZATION 9

Particle Swarm Optimization: Introduction – Principles of bird flocking and fish schooling – Evolution of PSO – Operating principles – PSO Algorithm – Neighborhood Topologies – Convergence criteria – Applications of PSO, Honey Bee Social Foraging Algorithms, Bacterial Foraging Optimization Algorithm.

TOTAL : 45 PERIODS

OUTCOMES:

Upon completion of the course, students will be able to:

- Design of the fundamental Computational Intelligence models
- Apply the concepts of neural networks, genetic algorithms, fuzzy neural networks, and ant colony optimization algorithms
- Application of computational Intelligence techniques to classification, pattern recognition, prediction, rule extraction, and optimization problems.

REFERENCES:

1. Christopher M. Bishop, "Neural Networks for Pattern Recognition", Oxford University Press
2. Nello Cristianini, John Shawe-Taylor, "An Introduction to Support Vector Machines and Other Kernel-based Learning Methods",Cambridge University Press.
3. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani," Neuro-fuzzy and soft computing: a computational approach to learning and machine intelligence", Prentice Hall of India, New Delhi. H.-J. Zimmermann, "Fuzzy Set Theory and its Applications", Springer.
4. David E. Goldberg, "Genetic Algorithms in search, Optimization & Machine Learning", Pearson Education.
5. Kenneth A DeJong,"Evolutionary Computation A Unified Approach", Prentice Hall of India, New Delhi.
6. Marco Dorigo and Thomas Stutzle, "Ant Colony optimization", Prentice Hall of India, New Delhi.
7. N P Padhy, Artificial Intelligence and Intelligent Systems, Oxford University Press, 2005
8. Engelbrecht, A.P. Fundamentals of Computational Swarm Intelligence, Wiley.

AP 7073 DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS L T P C
3 0 0 3

OBJECTIVES:

- Discusses the algorithmic complexity parameters and the basic algorithmic design techniques.
- To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms and NP Hard Problems.

UNIT I INTRODUCTION 9

Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II DESIGN TECHNIQUES 9

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III SEARCHING AND SORTING 9

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

UNIT IV GRAPH ALGORITHMS 9

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms,max-flow min cut theorem, Steiglitz's link deficit algorithm.

UNIT V SELECTED TOPICS 9

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

TOTAL : 45 PERIODS

OUTCOMES:

- Will be able to apply the suitable algorithm according to the given optimization problem.
- Ability to modify the algorithms to refine the complexity parameters.

REFERENCES:

1. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley, 1988.
2. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994.
3. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988.
4. D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley, 1989.

AP 7076 HARDWARE AND SOFTWARE CO DESIGN L T P C
3 0 0 3

Objectives:

- The students will learn various design steps starting from system specifications to hardware/software implementation and will experience process optimization while considering various design decisions.
- Students will gain design experience with project/case studies using contemporary high-level methods and tools.

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems , Hardware/Software Co-Design , Co-Design for System Specification and Modelling Co-Design for Heterogeneous Implementation - Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification .

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph , Formulation of the HW/SW Partitioning Problem , Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms .

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification , Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation

TOTAL : 45 PERIODS

OUTCOMES:

On completion of the course, a student should be able:

- To outline and apply design methodologies
- To appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their inter-relationships
- To modern hardware/software tools for building prototypes
- To demonstrate practical competence in these areas.

REFERENCES:

1. Ralf Niemann , “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup , Wayne Wolf ,”Hardware/Software Co-Design: Principles and Practice” , Kluwer Academic Pub,1997.
3. Giovanni De Micheli , Rolf Ernst Morgon,” Reading in Hardware/Software Co-Design “ Kaufmann Publishers,2001.

AP 7077 INTRODUCTION TO MEMS SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To give them hands on experience for the fabrication processes using micro-fabrication tools in the cleanroom.
- Briefly review on various application fields of the microsensors, MEMS, and smart devices. The materials and the processes required to make different kinds of the microdevices.
- The standard microelectronics technology to produce ultra large-scale integrated circuits and package them will also be reviewed. The new techniques that have been developed to make microsensors and microactuators, such as bulk and surface silicon micromachining will be followed.
- The fabrication process will include metal thin film e-beam evaporation, dielectric thin film growing using oxidation tube furnace, electrochemical deposition, and various kinds of chemical processes.

UNIT I INTRODUCTION TO MEMS 9

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelorometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II MECHANICS FOR MEMS DESIGN 9

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III ELECTRO STATIC DESIGN 9

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV CIRCUIT AND SYSTEM ISSUES 9

Electronic Interfaces, Feed back systems, Noise , Circuit and system issues, Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

UNIT V INTRODUCTION TO OPTICAL AND RF MEMS 9

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

TOTAL : 45 PERIODS

OUTCOMES:

On completion of the module students should:

- Be able to extend the principles of microfabrication to the development of micromechanical devices and the design of microsystems
- Understand the principles of energy transduction, sensing and actuation on a microscopic scale.
- Appreciate the effects of scaling, and the similarities and differences between micromechanical assemblies and macroscopic machines.
- Be able to analyse and model the behaviour of microelectromechanical devices and systems

TEXT BOOK:

1. Stephen Santuria," Microsystems Design", Kluwer publishers, 2000.

REFERENCES:

1. Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000
2. Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton,2000.
3. Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

AP 7078 NONLINEAR SIGNAL PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To introduce nonlinear filtering concepts, algorithms and architectures
- To apply these algorithms in Image processing

UNIT I INTRODUCTION TO NONLINEAR FILTERS AND STATISTICAL PRELIMINARIES 8

Nonlinear filters – measure of robustness – M estimators – L estimators – R estimators – order statistics – median filter and their characteristics – impulsive noise filtering by median filters – Recursive and weighted median filters – stock filters.

UNIT II NON LINEAR DIGITAL SIGNAL PROCESSING BASED ON ORDER STATISTICS 7

Time ordered nonlinear filters – rank ordered nonlinear filters – max/median filtering – median hybrid filters – characteristics of ranked order filters – L filters – M filters – R filters – comparison.

UNIT III ADAPTIVE NONLINEAR AND POLYNOMIAL FILTERS 10

Definition of polynomial filters – Wiener filters – robust estimation of scale – Adaptive filter based on local statistics – Decision directed filters – Adaptive L filters – Comparison of adaptive nonlinear filters – Neural networks for nonlinear filter

UNIT IV ALGORITHMS AND ARCHITECTURES 10

Sorting and selection algorithm – running median algorithm – fast structures for median and order statistics filtering – systolic array implementation – Wave front array implementation – quadratic digital filters implementation

UNIT V APPLICATIONS OF NONLINEAR FILTERS 10

Power spectrum analysis – Morphological image processing – nonlinear edge detection impulse noise rejection in image and bio signals – two component image filtering – speech processing

TOTAL : 45 PERIODS

OUTCOMES:

- Prepare and apply the optimal solution to the filtering problem
- Ability to solve linear and nonlinear filtering problem as applied to signal and image processing

REFERENCES:

1. Loannis Pitas, Anastarios, N.Venetsanopoulos, Nonlinear Digital filters –
2. Principles and Applications Kluwer Academic Publishers, 1990
3. Jaakko T.Astola, Jaakko Astola Kuosmanen, Fundamentals of Nonlinear Digital filtering , CRC Press LLC, 1997
4. Wing Kuen Ling, Nonlinear Digital filters: Analysis and Applications , Elsevier Science & Tech. 2007
5. GonzaloR. Arce, Nonlinear Signal Processing – A statistical approach , Wiley Publishers, 2005

VL 7080 SELECTED TOPICS IN ASIC DESIGN **L T P C**
3 0 0 3

OBJECTIVES:

- The course focuses on the semi custom IC Design and introduces the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles.
- The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN **9**

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS **9**

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECUTRE **9**

Architecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING **9**

Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.

UNIT V HIGH PERFORMANCE ALGORITHMS FOR ASICS/ SOCS. SOC CASE STUDIES **9**

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL: 45 PERIODS

OUTCOMES:

After completing this course:

- The student would have gained knowledge in the circuit design aspects at the next transistor and block level abstractions of FPGA and ASIC design. In combination with the course on CAD for VLSI, the student would have gained sufficient theoretical knowledge for carrying out FPGA and ASIC designs.

REFERENCES:

1. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2003
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science.
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation of Signal Processing Systems”, Wiley, 2008
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. Douglas J. Smith, *HDL Chip Design*, Madison, AL, USA: Doone Publications, 1996.
6. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994

AP 7081 **SELECTED TOPICS IN IC DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- This course deals with the supply circuit modules which are crucial modules in an IC design. Clock generation circuits play a major role in High Speed Broad Band Communication circuits, High Speed I/O's, Memory modules and Data Conversion Circuits.
- This course focuses on the design aspect of Clock Generation circuits and their design constraints.

UNIT I VOLTAGE AND CURRENT REFERENCES 9

Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II LOW DROP OUT REGULATORS 9

Analog Building Blocks, Negative Feedback, AC Design, Noise and Noise Reduction Techniques, Stability, LDO Efficiency, LDO Current Source, LDO Current Source Using Opamp.

UNIT III OSCILLATOR FUNDAMENTALS 9

General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator,Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for Ring Oscillators, Phase Noise in Differential LC Oscillators.

UNIT IV PHASE LOCK LOOPS 9

PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building blocks, Jitter and Phase Noise performance.

UNIT V CLOCK AND DATA RECOVERY 9

CDR Architectures, Tias and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL : 45 PERIODS

OUTCOMES:

This course provides the essential know how to a designer to construct Supply reference circuits and Clock Generation Circuits for given design specifications and aids the designer to understand the design specifications related to Supply and Clock Generation Circuits

REFERENCES:

1. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgap circuits",John wiley & Sons, Inc 2002.
2. Floyd M. Gardner ,"Phase LocK Techniques" John wiley & Sons, Inc 2005.
3. High Speed Clock and Data Recovery, High-performance Amplifiers Power Management " springer, 2008.
4. Behzad Razavi, " Design of Integrated circuits for Optical Communications", McGraw Hill, 2003.

AP 7082 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic,Common-mode current, differential-mode current , Connectors

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL : 45 PERIODS

OUTCOMES:

- Ability to identify sources affecting the speed of digital circuits.
- Able to improve the signal transmission characteristics.

REFERENCES

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR , 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handboo of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.

TOOLS REQUIRED

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

AP 7083 WIRELESS SENSOR NETWORKS L T P C
3 0 0 3

OBJECTIVES:

- To enable the student to understand the role of sensors and the networking of sensed data for different applications.
- To expose the students to the sensor node essentials and the architectural details, the medium access and routing issues and the energy constrained operational scenario.
- To enable the student to understand the challenges in synchronization and localization of sensor nodes, topology management for effective and sustained communication, data management and security aspects.

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9

Challenges for Wireless Sensor Networks-Characteristics requirements-required mechanisms, Difference between mobile ad-hoc and sensor networks, Applications of sensor networks- case study, Enabling Technologies for Wireless Sensor Networks.

UNIT II ARCHITECTURES 9

Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes , Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concepts. Physical Layer and Transceiver Design Considerations

UNIT III MAC AND ROUTING 9

MAC Protocols for Wireless Sensor Networks, IEEE 802.15.4, Zigbee, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing.

UNIT IV INFRASTRUCTURE ESTABLISHMENT 9

Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT V DATA MANAGEMENT and SECIRUTY 9

Data management in WSN, Storage and indexing in sensor networks, Query processing in sensor, Data aggregation, Directed diffusion, Tiny aggregation, greedy aggregation, security in WSN.

TOTAL : 45 PERIODS

OUTCOMES:

- The student would be able to appreciate the need for designing energy efficient sensor nodes and protocols for prolonging network lifetime.
- The student would be able to demonstrate an understanding of the different implementation challenges and the solution approaches.

REFERENCES

1. Ian F. Akyildiz, Mehmet Can Vuran, “ Wireless Sensor Networks” John Wiley, 2010
2. Yingshu Li, My T. Thai,Weili Wu, “ Wireless Sensor Networks and Applications” Springer 2008
3. Holger Karl & Andreas Willig, " Protocols And Architectures for Wireless Sensor Networks" , John Wiley, 2005.
4. Feng Zhao & Leonidas J. Guibas, “Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
5. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks-s Technology, Protocols, And Applications”, John Wiley, 2007.
6. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.
7. Bhaskar Krishnamachari, ”Networking Wireless Sensors”, Cambridge Press,2005.
8. Mohammad Ilyas And Imad Mahgaob,”Handbook Of Sensor Networks: Compact Wireless And Wired Sensing Systems”, CRC Press,2005.
9. Wayne Tomasi, “Introduction To Data Communication And Networking”, Pearson Education, 2007.

VL 7252 **LOW POWER VLSI DESIGN** **LT P C**
3 0 0 3

OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

UNIT IV POWER ESTIMATION 9

Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES:

- The student will apply the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

REFERENCES

1. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer, 2002.
3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons, inc. 2001.

VL 7071 SOLID STATE DEVICE MODELING AND SIMULATION L T P C
3 0 0 3

OBJECTIVES:

- The three areas of circuit design, device modeling and CAD tools are the main pillars based on which all VLSI system designs are carried out.
- This course introduces the principles of device modeling wherein device physics and experimentally observed device performance characteristics combined so as to lead to predictable equations and expressions for device performance under various scenarios of excitation.
- The most widely used device models used by the industry including BSIM and EKV models discussed.

UNIT I MOSFET DEVICE PHYSICS 9

Band theory of solids, carrier transport mechanism, MOS capacitor - surface potential, accumulation, depletion, inversion, electrostatic potential and charge distribution, threshold voltage, polysilicon work function, interface states and oxide traps, drain current model, sub-threshold characteristics.

UNIT II MOSFET MODELING 9

Basic modeling, SPICE Level-1, 2 and 3 models, Short channel effects, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling.

UNIT III NOISE MODELING 9

Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuit .

UNIT IV BSIM4 MOSFET MODELING 9

Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, Mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, Noise model, Junction diode models , Layout-dependent parasitics model.

UNIT V OTHER MOSFET MODELS 9

The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, Noise model, temperature effects, MOS model 9, MOSAI model, PSP model, Influence of process variation, Modeling of device mismatch for Analog/RF Applications.

TOTAL: 45 PERIODS

OUTCOMES:

The student who completes this course will be in a position understand the procedures used to construct the complicated device models that are widely used in VLSI CAD tools.

As the CMOS technology progresses, the student will be in a position to understand the changes introduced in the device models as well as contribute to the development of appropriate device models.

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly, Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd.
2. B. G. Streetman and S. Banarjee, “Solid State Electronic Devices”, Prentice-Hall of India Pvt. Ltd, New Delhi, India.
3. A. B. Bhattacharyya, “Compact MOSFET Models for VLSI Design”, John Wiley & Sons Inc., 2009.

VL 7072 TESTING OF VLSI CIRCUITS LT P C
3 0 0 3

OBJECTIVES:

- In the VLSI design industry, a significant portion of work force and resources are been deployed in the test and validation of VLSI designs. The complexity of multimillion transistor based VLSI deign calls for special techniques for efficiently testing and validating the VLSI design across all possible input, supply, speed and process corners. This has given rise to systematic areas of study in the form of design for test, automatic test pattern generation, fault diagnosis and these have all become very important areas from both research as well as routine industrial practice point of view.
- The present course will introduce the student to the mathematical and scientific principles based on which systematic test and validation can be carried out on multimillion transistor VLSI design.

UNIT I BASICS OF TESTING AND FAULT MODELLING 9

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.

UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches.

UNIT IV SELF-TEST AND TEST ALGORITHMS 9

Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

TOTAL : 45 PERIODS

OUTCOMES:

- The student who completes this course will be familiar with the principles used in the construction VLSI Design For Test (DFT) tools.
- The student will be able to adapt these to his specific industrial needs, also contribute to the development of more efficient tools from the fault overage and speed point of view.

REFERENCES:

1. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4. A.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems",
5. Prentice Hall International, 2002.

VL 7073 **VLSI SIGNAL PROCESSING** **L T P C**
3 0 0 3

OBJECTIVES:

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL : 45 PERIODS

OUTCOMES:

- Ability to modify the existing or new DSP architectures suitable for VLSI Implementation

REFERENCES

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

VL 7151 **CAD FOR VLSI CIRCUITS** **L T P C**
3 0 0 3

OBJECTIVES:

- The design of all VLSI circuits is carried out by making extensive use Computer Aided Design (CAD) VLSI design tool. Due to continuous scaling of semiconductor technology, most of the VLSI designs employ millions of transistors and circuits of this size can only be carried out with the aid of CAD VLSI design tools.
- The VLSI design professional needs to have a good understanding of the operation of these CAD VLSI design tools as these are developed primarily for and by the VLSI design professionals.
- As part of the present introductory course the principles of operation of all the important modules that go into the construction of a complete VLSI CAD tool will be discussed. These include the design flow organization for VLSI, the standard cell based synthesis methodologies for digital VLSI, floor planning and placement principles and related topics will be covered.

UNIT I VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III FLOOR PLANNING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS 9

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Use VLSI design automation tools
- Perform high level synthesis
- Discuss floor planning concepts
- Design algorithms for placement and partitioning

REFERENCES

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

VL 7251 **DATA CONVERTERS** **L T P C**
3 0 0 3

OBJECTIVES:

- Analog to Digital (AD) and Digital to Analog (DA) converters constitute a very important building block in all electronics systems. It is these blocks which provide the crucial interface between the primarily analog real world signals and the predominantly digital electronic systems.
- These are critical blocks which are utilized in all major industrial sectors including computers, wireless communication, audio and video systems, biomedical systems, aerospace and automotive systems and so on. There are a few established circuit architectures and principles for design of AD and DA converters.
- The performance limits of both these blocks have been continuously and rapidly improved upon over the last thirty years and this trend is expected to continue at the same pace in the foreseeable future too.
- The present course will explain the basic operational and design principles of the most important CMOS AD and DA converter architectures.

UNIT I INTRODUCTION AND CHARACTERISTICS OF AD/DA CONVERTER CHARACTERISTICS 9

Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and antialiasing filters.

UNIT II SWITCH CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques

UNIT III NYQUIST RATE D/A CONVERTERS 9

Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues in current element matching, clock feedthrough, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs

UNIT IV PIPELINE AND OTHER ADCs 9

Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V SIGMA DELTA CONVERTERS 9

STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Opamp nonlinearities,

TOTAL: 45 PERIODS

OUTCOMES:

- The student who undergoes this course will be able to carry out the design calculations for developing the various blocks associated with a typical CMOS AD or DA converter, select an appropriate configuration as per the required specifications on overall converter, and eventually arrive at the dimensions and bias conditions of all the MOS transistors involved in the design.

REFERENCES:
1. Behzad Razavi, “Principles of data conversion system design”, IEEE press, 1995.
2. M. Pelgrom, Analog-to-Digital Conversion, Springer, 2010.
3. Rudy van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters” Kluwer Acedamic Publishers, Boston, 2003.
4. R. Schreier, G. Temes, Understanding Delta-Sigma DataConverters, Wiley-IEEE Press, 2004
5. J. G. Proakis, D. G. Manolakis, Digital Signal Processing Principles, Algorithms and Applications 4th Edition Prentice Hall, 2006.
6. VLSI Data Conversion Circuits EE658 recorded lectures available at http://www.ee.iitm.ac.in/~nagendra/videolecture

AP 7001 ADVANCED COMPUTER ARCHITECTURE DESIGN **L T P C**
3 0 0 3

OBJECTIVES:
- To Illustrate, with suitable examples, the concepts and principles of parallel processing.
- To make the students familiarize with modern processor technology and the supporting memory hierarchy.
- To introduce and study the system architecture with parallel, vector and scalable architecture for building high-performance computers

UNIT I THEORY OF PARALLELISM 9
Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.

UNIT II PARTITIONING AND SCHEDULING 9
Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

UNIT III HARDWARE TECHNOLOGIES 9
Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory – Bus Arbitration, cache memory organisations, shared memory organisations, sequential and weak consistency models.

UNIT IV PIPELINING, SUPERSCALAR , PARALLEL AND SCALABLE ARCHITECTURE 9
Linear and Non-Linear Pipeline processor – Instruction and Arithmetic Pipeline Design – Supescalar and Superpipeline Design – Multiprocessor Interconnects – Cache Coherence and Synchronization mechanism – Message Passing Mechanism – Flow Control Strategies – Multicast Routing Strategies

UNIT V MULTIVECTOR AND SIMD COMPUTERS 9
Vector processing Principles – Compund Vector Processing – SIMD Computer Organisation – Synchronized MIMD machine – Latency Hiding Technique – Multithreading –Scalable and and Multithreaded Architectures – Data Flow and Hybrid Architectures - Parallel models, Languages and compilers, Parallel program development and environments.

TOTAL : 45 PERIODS

OUTCOMES:

- Able to explain the advanced concepts of parallel architecture
- Apply the memory hierarchy for multiprocessor system
- Able to analyze the design structures of pipelined and multiprocessor systems

REFERENCES

1. Kai Hwang, " Advanced Computer Architecture ", McGraw Hill International, 2001.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, ”Advanced Computer architecture – A design Space Approach” , Pearson Education , 2003.
3. John P.Shen, “Modern processor design . Fundamentals of super scalar processors”, Tata McGraw Hill 2003.
4. Kai Hwang, “Scalable parallel computing”, Tata McGraw Hill 1998.
5. William Stallings, “ Computer Organization and Architecture”, Macmillan Publishing Company, 1990.
6. M.J. Quinn, “ Designing Efficient Algorithms for Parallel Computers”, McGraw Hill International, 1994.
7. Barry, Wilkinson, Michael, Allen “Parallel Programming”, Pearson Education Asia , 2002
8. Harry F. Jordan Gita Alaghband, “ Fundamentals of parallel Processing”, Pearson Education , 2003
9. Richard Y.Kain, “ Advanced computer architecture –A systems Design Approach”, PHI, 2003.

AP 7075 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN **L T P C**
3 0 0 3

OBJECTIVES:

- To understand the concepts related to Electromagnetic interference in PCBs
- To provide solutions for minimizing EMI in PCBs
- To learn EMI standards in the design of PCBs
- To learn various EMI coupling principles, EMI standards and measurements
- To provide knowledge on EMI control techniques and design procedures to make EMI compatible PCBs

UNIT I EMI/EMC CONCEPTS 9

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES 9

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES 9

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS 9

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS 9

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL : 45 PERIODS

OUTCOMES:

- Analyze Electromagnetic interference effects in PCBs
- Propose solutions for minimizing EMI in PCBs
- Analyze Electromagnetic environment, EMI coupling, standards, measurement and control techniques

REFERENCES:

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork, 1996.
2. Henry W.Ott.,"Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3. Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, Norwood, 1986.
4. C.R.Paul,"Introduction to Electromagnetic Compatibility" , John Wiley and Sons, Inc, 1992.
5. Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC" , Vol I-V, 1988.

AP 7079 RF SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- The CMOS RF Front End (RFE) is a very crucial building block and in all of wireless and many high frequency wire-line systems. The RFE has few important building blocks within including the Low Noise Amplifiers, Phase Locked Loop Synthesizers, Mixers, Power Amplifiers, and impedance matching circuits.
- The present course will introduce the principles of operation and design principles associated with these important blocks.
- The course will also provide and highlight the appropriate digital communication related design objectives and constraints associated with the RFEs

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES 9

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT IV MIXERS AND OSCILLATORS 9

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS 9

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TOTAL : 45 PERIODS

OUTCOMES:

- The student after completing this course must be able to translate the top level wireless communications system specifications into block level specifications of the RFE.
- The student should also able to carry out transistor level design of the entire RFE.

TEXT BOOKS

1. T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004.
2. B.Razavi, "RF Microelectronics", Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, 1997.
4. B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001
5. Recorded lectures and notes available at. http://www.ee.iitm.ac.in/~ani/ee6240/

AP 7074 DSP INTEGRATED CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To familiarize the concept of DSP and DSP algorithms.
- Introduction to Multirate systems and finite wordlength effects
- To know about the basic DSP processor architectures and the synthesis of the processing elements
- To gather an idea about the VLSI circuit layout design styles.

UNIT I INTRODUCTION TO DSP INTEGRATED CIRCUITS 9

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT III DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. TMS320C54x and TMS320C6x architecture, Motorola DSP56002 architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES AND ARITHMETIC UNIT 9

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

Arithmetic Unit : Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator.

UNIT V CASE STUDY-INTEGRATED CIRCUIT DESIGN 9

Layout of VLSI circuits, Layout Styles, Case Study : FFT processor, DCT processor and Interpolator.

TOTAL: 45 PERIODS

OUTCOMES:

- Get to know about the Digital Signal Processing concepts and it's algorithms
- Get an idea about finite wordlength effects in digital filters
- Concept behind multirate systems is understood.
- Get familiar with the DSP processor architectures and how to perform synthesis of processing elements
- Acquire an general idea about VLSI circuit layout design aspects

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1. Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 1999.
2. John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education, 2002.
3. B.Venkatramani, M.Bhaskar, "Digital Signal Processors", Tata McGraw-Hill, 2002.
4. Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital signal processing – A practical approach", Tata McGraw-Hill, 2002.
5. Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.