# UNIVERSITY DEPARTMENTS

## ANNA UNIVERSITY CHENNAI : : CHENNAI 600 025

## REGULATIONS - 2009

## CURRICULUM I TO IV SEMESTERS (FULL TIME)

# M.E. APPLIED ELECTRONICS

### SEMESTER I

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| **THEORY** | | | | | | |
| 1 | MA9109 | Applied Mathematics for Electronics Engineers | 3 | 1 | 0 | 4 |
| 2 | AP9111 | Advanced Digital System Design | 3 | 0 | 0 | 3 |
| 3 | AP9112 | Digital CMOS VLSI Design | 3 | 0 | 0 | 3 |
| 4 | AP9113 | Analog Integrated Circuit Design | 3 | 0 | 0 | 3 |
| 5 | AP9114 | Statistical Signal Processing | 3 | 0 | 0 | 3 |
| 6 | E1 | Elective I | 3 | 0 | 0 | 3 |
| **PRACTICAL** | | | | | | |
| 7 | AP9117 | Embedded Systems Design Laboratory | 0 | 0 | 4 | 2 |
| | | **TOTAL** | **18** | **0** | **4** | **21** |

### SEMESTER II

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| **THEORY** | | | | | | |
| 1 | AP9122 | Digital Image Processing | 3 | 0 | 0 | 3 |
| 2 | AP9121 | Advanced Control Engineering | 3 | 0 | 0 | 3 |
| 3 | E2 | Elective II | 3 | 0 | 0 | 3 |
| 4 | E3 | Elective III | 3 | 0 | 0 | 3 |
| 5 | E4 | Elective IV | 3 | 0 | 0 | 3 |
| 6 | E5 | Elective V | 3 | 0 | 0 | 3 |
| **PRACTICAL** | | | | | | |
| 7 | AP9124 | Integrated Circuits Design Laboratory | 0 | 0 | 4 | 2 |
| | | **TOTAL** | **18** | **0** | **4** | **20** |

**SEMESTER III**

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| **THEORY** | | | | | | |
| 1 | E6 | Elective VI | 3 | 0 | 0 | 3 |
| 2 | E7 | Elective VII | 3 | 0 | 0 | 3 |
| 3 | E8 | Elective VIII | 3 | 0 | 0 | 3 |
| **PRACTICAL** | | | | | | |
| 4 | AP9135 | Project Work – Phase I | 0 | 0 | 12 | 6 |
| | | **TOTAL** | **9** | **0** | **12** | **15** |

**SEMESTER IV**

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| **PRACTICAL** | | | | | | |
| 1 | AP9141 | Project Work – Phase II | 0 | 0 | 24 | 12 |
| | | **TOTAL** | **0** | **0** | **24** | **12** |

**TOTAL CREDITS TO BE EARNED FOR THE AWARD OF DEGREE = 68**

# UNIVERSITY DEPARTMENTS

## ANNA UNIVERSITY CHENNAI : : CHENNAI 600 025

## REGULATIONS - 2009

## CURRICULUM I TO VI SEMESTERS (PART TIME)

# M.E. APPLIED ELECTRONICS

**SEMESTER I**

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| **THEORY** | | | | | | |
| 1. | MA9109 | Applied Mathematics for Electronics Engineers | 3 | 1 | 0 | 4 |
| 2. | AP9111 | Advanced Digital System Design | 3 | 0 | 0 | 3 |
| 3. | AP9112 | Digital CMOS VLSI Design | 3 | 0 | 0 | 3 |
| | | **TOTAL** | **9** | **1** | **0** | **10** |

**SEMESTER II**

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| **THEORY** | | | | | | |
| 1. | AP9122 | Digital Image Processing | 3 | 0 | 0 | 3 |
| 2. | AP9121 | Advanced Control Engineering | 3 | 0 | 0 | 3 |
| 3. | E1 | Elective I | 3 | 0 | 0 | 3 |
| | | **TOTAL** | **9** | **0** | **0** | **9** |

**SEMESTER III**

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| **THEORY** | | | | | | |
| 1. | AP9113 | Analog IC Design | 3 | 0 | 0 | 3 |
| 2. | AP9114 | Statistical Signal Processing | 3 | 0 | 0 | 3 |
| 3. | E2 | Elective II | 3 | 0 | 0 | 3 |
| **PRACTICAL** | | | | | | |
| 4. | AP9117 | Embedded Systems Design Laboratory | 0 | 0 | 4 | 2 |
| | | **TOTAL** | **9** | **0** | **4** | **11** |

**SEMESTER IV**

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| **THEORY** | | | | | | |
| 1. | E3 | Elective III | 3 | 0 | 0 | 3 |
| 2. | E4 | Elective IV | 3 | 0 | 0 | 3 |
| 3. | E5 | Elective V | 3 | 0 | 0 | 3 |
| **PRACTICAL** | | | | | | |
| 4. | AP9124 | Integrated Circuits Design Laboratory | 0 | 0 | 4 | 2 |
| | | **TOTAL** | **9** | **0** | **4** | **11** |

**SEMESTER V**

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| **THEORY** | | | | | | |
| 1. | E6 | Elective VI | 3 | 0 | 0 | 3 |
| 2. | E7 | Elective VII | 3 | 0 | 0 | 3 |
| 3. | E8 | Elective VIII | 3 | 0 | 0 | 3 |
| **PRACTICAL** | | | | | | |
| 4. | AP9135 | Project Work – Phase I | 0 | 0 | 12 | 6 |
| | | **TOTAL** | **9** | **0** | **12** | **15** |

**SEMESTER VI**

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| **PRACTICAL** | | | | | | |
| 1. | AP9141 | Project Work – Phase II | 0 | 0 | 24 | 12 |
| | | **TOTAL** | **0** | **0** | **24** | **12** |

**TOTAL NO.OF CREDITS TO BE EARNED FOR THE AWARD OF DEGREE=68**

**LIST OF ELECTIVES**

| SL. NO | COURSE CODE | COURSE TITLE | L | T | P | C |
|---|---|---|---|---|---|---|
| 1 | CP9162 | ASIC Design | 3 | 0 | 0 | 3 |
| 2 | AP9151 | Neural Networks and Its Applications | 3 | 0 | 0 | 3 |
| 3 | AP9152 | Hardware Software Co-Design. | 3 | 0 | 0 | 3 |
| 4 | AP9153 | Signal Integrity for high speed design | 3 | 0 | 0 | 3 |
| 5 | AP9154 | Computer Architecture | 3 | 0 | 0 | 3 |
| 6 | CP9163 | Embedded systems | 3 | 0 | 0 | 3 |
| 7 | AP9155 | Electromagnetic Interference and Compatibility in System Design | 3 | 0 | 0 | 3 |
| 8 | AP9159 | Power Electronics | 3 | 0 | 0 | 3 |

| | | | | | | |
|---|---|---|---|---|---|---|
| 9 | VL9111 | CAD for VLSI circuits | 3 | 0 | 0 | 3 |
| 10 | AP9156 | Design and Analysis of Algorithms | 3 | 0 | 0 | 3 |
| 11 | AP9157 | Selected Topics in IC design | 3 | 0 | 0 | 3 |
| 12 | AP9158 | Internet working and Multimedia | 3 | 0 | 0 | 3 |
| 13 | AP9166 | VLSI Signal Processing. | 3 | 0 | 0 | 3 |
| 14 | CU9122 | RF System design | 3 | 0 | 0 | 3 |
| 15 | AP9160 | Synthesis and Optimization of Digital Circuits | 3 | 0 | 0 | 3 |
| 16 | AP9161 | Data Converters | 3 | 0 | 0 | 3 |
| 17 | AP9162 | Advanced microprocessors and microcontrollers | 3 | 0 | 0 | 3 |
| 18 | AP9163 | Introduction to MEMS System Design | 3 | 0 | 0 | 3 |
| 19 | AP9164 | High Speed Switching Architectures | 3 | 0 | 0 | 3 |
| 20 | AP9165 | Wireless sensor networks | 3 | 0 | 0 | 3 |
| 21 | | Special Elective | 3 | 0 | 0 | 3 |

**MA9109 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS**

| L | T | P | C |
|---|---|---|---|
| 3 | 1 | 0 | 4 |

**UNIT I FUZZY LOGIC 9**

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

**UNIT II MATRIX THEORY 9**

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications.

**UNIT III ONE DIMENSIONAL RANDOM VARIABLES 9**

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform,

Exponential, Gamma and Normal distributions – Function of a Random Variable.

**UNIT IV DYNAMIC PROGRAMMING 9**

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

**UNIT V QUEUEING MODELS 9**

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

**TOTAL (L: 45+T: 15): 60 PERIODS**

**REFERENCES:**


1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000.
3. Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 7th Edition, Prentice – Hall of India, Private Ltd., New Delhi (2007).
4. Taha, H.A., Operations Research, An introduction, 7th edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, Fundamentals of Queueing theory, 2nd edition, John Wiley and Sons, New York (1985).

**AP9111 ADVANCED DIGITAL SYSTEM DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**UNIT I SEQUENTIAL CIRCUIT DESIGN 9**

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits-design of iterative circuits-ASM chart and realization using ASM

**UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9**

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

**UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9**

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

**UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9**

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

**UNIT V SYSTEM DESIGN USING VHDL 9**

VHDL operators – Arrays – concurrent and sequential statements – packages- Data flow – Behavioral – structural modeling – compilation and simulation of VHDL code –Test bench - Realization of combinational and sequential circuits using HDL – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

**TOTAL : 45 PERIODS**

**REFERENCES**


1 Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004
2 Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001
3 Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
4 Parag K.Lala “Digital system Design using PLD” B S Publications,2003
5 Charles H Roth Jr.”Digital System Design using VHDL” Thomson learning, 2004
6 Douglas L.Perry “VHDL programming by Example” Tata McGraw.Hill - 2006

**AP9112 DIGITAL CMOS VLSI DESIGN**

**L T P C**
**3 0 0 3**

**UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9**

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

**UNIT II INVERTERS AND LOGIC GATES. 9**

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

**UNIT III CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 9**

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

**UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN. 9**

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling ,cross talk, floor planning, power distribution. Clock distribution.

**UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE 9**

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

**TOTAL : 45 PERIODS**

**REFERENCES**


1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2. John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc., 2002.
3. Samir Palnitkar, “Verilog HDL”, Pearson Education, 2nd Edition, 2004.
4. Eugene D.Fabricius, “Introduction to VLSI Design”, McGraw Hill International Editions, 1990.
5. J.Bhasker, B.S.Publications, “A Verilog HDL Primer”, 2nd Edition, 2001.
6. Pucknell, “Basic VLSI Design”, Prentice Hall of India Publication, 1995.
7. Wayne Wolf “Modern VLSI Design System on chip. Pearson Education.2002.

**AP9113 ANALOG INTEGRATED CIRCUIT DESIGN**

**L T P C**
**3 0 0 3**

**UNIT I SINGLE STAGE AMPLIFIERS 9**

Common source stage, Source follower, Common gate stage, Cascode stage, Single ended and differential operation, Basic differential pair, Differential pair with MOS loads

**UNIT II FREQUENCY RESPONSE AND NOISE ANALYSIS 9**

Miller effect ,Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascode stage, Differential pair, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

**UNIT III OPERATIONAL AMPLIFIERS 9**

Concept of negative feedback, Effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

**UNIT IV STABILITY AND FREQUENCY COMPENSATION 9**

General considerations, Multipole systems,Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

**UNIT V BIASING CIRCUITS 9**

Basic current mirrors, cascode current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

**TOTAL : 45 PERIODS**

**REFERENCES**


1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 2001
2. Grebene, “Bipolar and MOS Analog Integrated circuit design”, John Wiley & sons,Inc., 2003.
3. Willey Sansen
4. Phillip E.Allen, DouglasR.Holberg, “CMOS Analog Circuit Design”, Second edition, Oxford University Press, 2002

**AP9114 STATISTICAL SIGNAL PROCESSING**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9**

Discrete Random Processes- Ensemble Averages, Stationary processes, Bias and Estimation, Autocovariance, Autocorrelation, Parseval's theorem, Wiener-Khintchine relation, White noise, Power Spectral Density, Spectral factorization, Filtering Random Processes, Special types of Random Processes – ARMA, AR, MA – Yule-Walker equations.

**UNIT II SPECTRAL ESTIMATION 9**

Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric methods – ARMA, AR and MA model based spectral estimation, Solution using Levinson-Durbin algorithm

**UNIT III LINEAR ESTIMATION AND PREDICTION 9**

Linear prediction – Forward and Backward prediction, Solution of Prony's normal equations, Least mean-squared error criterion, Wiener filter for filtering and prediction, FIR and IIR Wiener filters, Discrete Kalman filter

**UNIT IV ADAPTIVE FILTERS 9**

FIR adaptive filters – adaptive filter based on steepest descent method- Widrow-Hopf LMS algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo cancellation, Adaptive noise cancellation, RLS adaptive algorithm.

**UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING 9**

Mathematical description of change of sampling rate – Interpolation and Decimation, Decimation by an integer factor, Interpolation by an integer factor, Sampling rate conversion by a rational factor, Polyphase filter structures, Multistage implementation of multirate system, Application to subband coding – Wavelet transform

**TOTAL (L: 45+T: 15): 60 PERIODS**

**REFERENCES**


1. Monson H. Hayes, 'Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc, Singapore, 2002
2. John J. Proakis, Dimitris G. Manolakis, : Digital Signal Processing', Pearson Education, 2002
3. Rafael C. Gonzalez, Richard E. Woods, " Digital Image Processing", Pearson Education Inc.,Second Edition, 2004 (For Wavelet Transform Topic)

**AP9117 EMBEDDED SYSTEMS DESIGN LABORATORY**

**L T P C**
**0 0 3 2**

1. Board development using 8051 microcontroller
2. Assembly and High level language programs for 8051 - ports – timers -Seven Segment display – UART – LCD interface
3. RTOS – Simple task creation, Round Robin Scheduling, Preemptive scheduling,
   Semaphores, Mailboxes.
4. Assembly and High level language programs for R8C - ports – timers -Seven Segment display – UART – LCD interface – Stepper Motor control
5. Assembly and High level language programs for MSP 430 - ports – timers - Seven Segment display – UART – LCD interface – Stepper Motor control

**AP9122 DIGITAL IMAGE PROCESSING**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**UNIT I DIGITAL IMAGE FUNDAMENTALS 9**

Elements of digital image processing systems, Vidicon and Digital Camera working principles, Elements of visual perception, brightness, contrast, hue, saturation, Mach Band effect, Image sampling, Quantization, Dither, Two dimensional mathematical preliminaries.

**UNIT II IMAGE TRANSFORMS 9**

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

**UNIT III IMAGE ENHANCEMENT AND RESTORATION 9**

Histogram modification, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contraharmonic and Yp mean filters . Design of 2D FIR filters. Image restoration - degradation model, Unconstrained and Constrained restoration, Inverse filtering-removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations-spatial transformations, Gray Level interpolation. .

**UNIT IV IMAGE SEGMENTATION AND RECOGNITION 9**

Image segmentation - Edge detection, Edge linking and boundary detection, Region growing, Region splitting and Merging, Image Recognition - Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation., Neural networks-Backpropagation network and training, Neural network to recognize shapes.

**UNIT V IMAGE COMPRESSION 9**

Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding, Transform coding, JPEG standard, JPEG 2000, EZW, SPIHT, MPEG.

**TOTAL : 45 PERIODS**

**REFERENCES:**


1. Rafael C. Gonzalez, Richard E. Woods, " Digital Image Processing", Pearson Education, Inc., Second Edition, 2004
2. Anil K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall of India, 2002.
3. Rafael C. Gonzalez, Richard E. Woods, Steven Eddins," Digital Image Processing using MATLAB", Pearson Education, Inc., 2004.
4. D.E. Dudgeon and R.M. Mersereau, "Multidimensional Digital Signal Processing", Prentice Hall Professional Technical Reference, 1990.

5. William K. Pratt, " Digital Image Processing", John Wiley, New York, 2002.
6. Milan Sonka et al, "Image Processing, Analysis and Machine Vision", Brookes/Cole, Vikas Publishing House, 2nd edition, 1999;
7. Sid Ahmed, M.A., " Image Processing Theory, Algorithms and Architectures", McGrawHill, 1995.

**AP9121 ADVANCED CONTROL ENGINEERING**

**L T P C**
**3 0 0 3**

**UNIT I PRINCIPLES OF CONTROLLERS 9**

Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

**UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9**

Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

**UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM 9**

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

**UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9**

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

**UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9**

Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

**TOTAL : 45 PERIODS**

**REFERENCES**

1. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.
2. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995.
3. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.

**AP9124 INTEGRATED CIRCUITS DESIGN LABORATORY**

| L | T | P | C |
|---|---|---|---|
| 0 | 0 | 3 | 2 |

1. Design Entry Using VHDL or Verilog, examples for circuit descriptions using HDL languages sequential and concurrent statements.
2. Structural and behavioral descriptions, principles of operation and limitation of HDL simulators. Examples of sequential and combinational logic design and simulation. Test vector generation.
3. CPLD – Board development. I/O interfacing, Analog interfacing, Real time application development.
4. FPGA- Board development. I/O interfacing, Analog interfacing, Real time application development.
5. System development using either PSPICE or FPGAs

**CP9162 ASIC DESIGN**

**L T P C**
**3 0 0 3**

**UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9**

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture

**UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9**

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

**UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9**

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

**UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9**

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

**UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9**

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

**TOTAL : 45 PERIODS**

**REFERENCES:**


1. M.J.S .Smith, " Application - Specific Integrated Circuits " - Addison -Wesley Longman Inc., 1997.
2. Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, " Field Programmable Gate Arrays ", Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
6. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

**AP9151 NEURAL NETWORKS AND ITS APPLICATIONS**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**UNIT I INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS 9**

Neuro-physiology - General Processing Element - ADALINE - LMS learning rule - MADALINE - MR2 training algorithm.

**UNIT II BPN AND BAM 9**

Back Propagation Network - updating of output and hidden layer weights -application of BPN – associative memory - Bi-directional Associative Memory - Hopfield memory - traveling sales man problem.

**UNIT III SIMULATED ANNEALING AND CPN 9**

Annealing, Boltzmann machine - learning - application - Counter Propagation network - architecture -training - Applications.

**UNIT IV SOM AND ART 9**

Self organizing map - learning algorithm - feature map classifier - applications - architecture of Adaptive Resonance Theory - pattern matching in ART network.

**UNIT V NEOCOGNITRON 9**

Architecture of Neocognitron - Data processing and performance of architecture of spacio - temporal networks for speech recognition.

**TOTAL : 45 PERIODS**

**REFERENCES:**

1. J.A. Freeman and B.M.Skapura , "Neural Networks, Algorithms Applications and Programming Techniques", Addison-Wesely,2003.

2. Laurene Fausett, "Fundamentals of Neural Networks: Architecture, Algorithms and Applications", Prentice Hall, 1994

**AP9152 HARDWARE - SOFTWARE CO-DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**UNIT I SYSTEM SPECIFICATION AND MODELLING 9**

Embedded Systems , Hardware/Software Co-Design , Co-Design for System Specification and Modelling , Co-Design for Heterogeneous Implementation - Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification .

**UNIT II HARDWARE/SOFTWARE PARTITIONING 9**

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph , Formulation of the HW/SW Partitioning Problem , Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms .

**UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS: 9**

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

**UNIT IV PROTOTYPING AND EMULATION 9**

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping ,Target Architecture-Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

**UNIT V DESIGN SPECIFICATION AND VERIFICATION 9**

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification , Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation

**TOTAL : 45 PERIODS**

**REFERENCES:**


1. Ralf Niemann , “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup , Wayne Wolf ,”Hardware/Software Co-Design: Principles and Practice” , Kluwer Academic Pub,1997.
3. Giovanni De Micheli , Rolf Ernst Morgon,” Reading in Hardware/Software Co-Design “ Kaufmann Publishers,2001.

**AP9153 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN**

**L T P C**
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**UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9**

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

**UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9**

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models

**UNIT III NON-IDEAL EFFECTS 9**

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic,Common-mode current, differential-mode current , Connectors

**UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9**

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis

**UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9**

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

**TOTAL : 45 PERIODS**

**REFERENCES**


1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR , 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handboo of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.


**TOOLS REQUIRED**

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

**AP9154 COMPUTER ARCHITECTURE**

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**UNIT I THEORY OF PARALLELISM 9**

Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.

**UNIT II PARTITIONING AND SCHEDULING 9**

Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

**UNIT III HARDWARE TECHNOLOGIES 9**

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory - backplane bus systems, cache memory organisations, shared memory organisations, sequential and weak consistency models.

**UNIT IV PIPELINING AND SUPERSCALAR TECHNOLOGIES 9**

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

**UNIT IV SOFTWARE AND PARALLEL PROGRAMMING 9**

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

**TOTAL : 45 PERIODS**

**REFERENCES**


1. Kai Hwang, " Advanced Computer Architecture ", McGraw Hill International, 2001.
2.. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer architecture – A design Space Approach" , Pearson Education , 2003.
3. John P.Shen, "Modern processor design . Fundamentals of super scalar processors", Tata McGraw Hill 2003.
4. Kai Hwang, "Scalable parallel computing", Tata McGraw Hill 1998.
5. William Stallings, " Computer Organization and Architecture", Macmillan Publishing Company, 1990.
6. M.J. Quinn, " Designing Efficient Algorithms for Parallel Computers", McGraw Hill International, 1994.
7. Barry, Wilkinson, Michael, Allen "Parallel Programming", Pearson Education Asia , 2002
8.Harry F. Jordan Gita Alaghband, " Fundamentals of parallel Processing", Pearson Education , 2003

9. Richard Y.Kain, " Advanced computer architecture –A systems Design Approach", PHI, 2003.

**CP9163 EMBEDDED SYSTEMS**

**L T P C**
**3 0 0 3**

**UNIT I EMBEDDED PROCESSORS 9**

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.

**UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM 9**

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture

**UNIT III NETWORKS 9**

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

**UNIT IV REAL-TIME CHARACTERISTICS 9**

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

**UNIT V SYSTEM DESIGN TECHNIQUES 9**

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

**TOTAL : 45 PERIODS**

**REFERENCES**

1. Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers.

2. Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia.
3. C. M. Krishna and K. G. Shin, “Real-Time Systems” , McGraw-Hill, 1997
4. Frank Vahid and Tony Givargis, “Embedded System Design: A Unified Hardware/Software Introduction” , John Wiley & Sons.
5. Product literature

**AP9155 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN**

**L T P C**
**3 0 0 3**

**UNIT I EMI/EMC CONCEPTS 9**

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

**UNIT II EMI COUPLING PRINCIPLES 9**

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

**UNIT III EMI CONTROL TECHNIQUES 9**

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

**UNIT IV EMC DESIGN OF PCBS 9**

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

**UNIT V EMI MEASUREMENTS AND STANDARDS 9**

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

**TOTAL : 45 PERIODS**

**REFERENCES**

1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996.
2. Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3rd Ed, Artech house, Norwood, 1986.

4. C.R.Paul,"Introduction to Electromagnetic Compatibility" , John Wiley and Sons, Inc, 1992.
5. Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC" , Vol I-V, 1988.

**AP9159 POWER ELECTRONICS**

**L T P C**
**3 0 0 3**

**UNIT I CONVERTERS IN EQUILIBRIUM 9**

Principles of Steady State Converter Analysis – Boost and Buck Converter Examples Steady-State Equivalent Circuit Modeling, Losses, and Efficiency – Equivalent circuit model – complete circuit model - - Switch Realization- Switching loss - Converter Circuits – Circuit manipulation – Transformer isolation – Converter evaluation and design

**UNIT II CONVERTER DYNAMICS AND CONTROL 9**

The Basic AC Modeling Approach - Averaging the Inductor and capacitor Waveforms - A Nonideal Flyback Converter - State-Space Averaging - Circuit Averaging and Averaged Switch Modeling - The Canonical Circuit Model - Converter Transfer Functions - Analysis of Converter Transfer Functions - Graphical Construction of Impedances and Transfer Functions - Controller Design - Input Filter Design- Current Programmed Control

**UNIT III MAGNETICS 9**

Basic Magnetics Theory - Transformer Modeling - Loss Mechanisms in Magnetic Devices - Eddy Currents in Winding Conductors - Inductor Design - Filter Inductor Design Constraints - A Step-by-Step Procedure - Transformer Design - A Step-by-Step Transformer Design Procedure

**UNIT IV MODERN RECTIFIERS AND POWER SYSTEM HARMONICS 9**

Power Phasors in Sinusoidal Systems - Harmonic Currents in Three-Phase Systems - AC Line Current Harmonic Standards - **Line-Commutated Rectifiers -** The Single-Phase Full-Wave Rectifier - The Three-Phase Bridge Rectifier - Phase Control - **Pulse-Width Modulated Rectifiers -** Realization of a Near-Ideal Rectifier - Control of the Current Waveform - Ideal Three-Phase Rectifiers

**UNIT IV RESONANT CONVERTERS 9**

**Resonant Conversion -** Sinusoidal Analysis of Resonant Converters – Examples - Soft Switching - Soft-Switching Mechanisms of Semiconductor Devices - The Zero-Current-Switching Quasi-Resonant Switch Cell - Resonant Switch Topologies - Soft Switching in PWM Converters

**REFERENCES**


1. Robert W. Erickson, Dragan Maksimovic," Fundamentals of Power Electronics", Kluwer Academic Publishers, Second Edition, New York, Boston, Dordrecht, London, Moscow.
2. Muhammad H Rashid, " Power Electronics – Circuits, Devices and Applications", Third Edition, Prentice Hall of India, 2004.
3. M.D. Singh, K.B.Khanchandani, " Power Electronics", Tata McGraw Hill, 1998.
4. Ned Mohan, Tore M Undeland, William P. Robbins, Power Electronics, Converters, Applications and Design", John Wiley & Sons, 1994.


**VL9111 CAD FOR VLSI CIRCUITS**

**L T P C**
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**UNIT I VLSI DESIGN METHODOLOGIES 9**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

**UNIT II DESIGN RULES 9**

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

**UNIT III FLOOR PLANNING 9**

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

**UNIT IV SIMULATION 9**

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

**UNIT V MODELLING AND SYNTHESIS 9**

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

**TOTAL : 45 PERIODS**

**REFERENCES**

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

**AP9156 DESIGN AND ANALYSIS OF ALGORITHMS**

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**UNIT I INTRODUCTION** **9**

Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

**UNIT II DESIGN TECHNIQUES** **9**

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

**UNIT III SEARCHING AND SORTING** **9**

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

**UNIT IV GRAPH ALGORITHMS** **9**

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms,max-flow min cut theorem, Steiglitz's link deficit algorithm.

**UNIT V SELECTED TOPICS** **9**

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

**TOTAL : 45 PERIODS**

**REFERENCES**

1. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley, 1988.
2. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994.
3. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia

Publications, 1988.
4. D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley, 1989.

**AP9157 SELECTED TOPICS IN IC DESIGN**

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**UNIT I VOLTAGE AND CURRENT REFERENCES 9**

PTAT current references, startup circuits and frequency compensation, CTAT current references, Temperature- independent current references, PTAT current generators, Voltage references, Zero-order references, first order references, Second-order references, state-of-the-Art Curvature-correction techniques.

**UNIT II PRECISION REFERENCE CIRCUITS 9**

Error source, The output stage, Designing for power supply rejection and line regulation, Effect of resistors temperature coefficient on a reference.

**UNIT III OSCILLATOR FUNDAMENTALS 9**

General considerations, Ring oscillators, LC oscillators, monolithic inductors, monolithic varactors, Quadrature oscillators, distributed oscillators, voltage controlled oscillators, mathematical model of VCOs.

**UNIT IV PHASE LOCKED LOOPS 9**

Basic PLL topology, Charge-Pump PLLs, nonideal effects in PLLs, Delay locked loops, Frequency multiplication and synthesis, skew reduction, Jitter reduction.

**UNIT V CLOCK AND DATA RECOVERY 9**

General considerations, Phase detectors for random data, frequency detectors for random data, Full rate referenceless architecture, Dual-VCO Architecture, Dual-loop architecture with external reference, jitter in CDR circuits.

**TOTAL : 45 PERIODS**

**REFERENCES**

1. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgap circuits",John wiley & Sons Inc.
2. Michiel Steyaert , Arthur H. M. van Roermund, Herman Casier "Analog Circuit Design High- speed Clock and Data Recovery, High-performance Amplifiers Power Management " Springer
3. Behzad Razavi, " Design of Integrated circuits for Optical Communications", Mc Graw Hill.

**AP9158 INTERNETWORKING AND MULTIMEDIA**

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**UNIT I MULTIMEDIA NETWORKING 9**

Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video.

**UNIT II BROAD BAND NETWORK TECHNOLOGY 9**

Broadband services, ATM and IP , IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance.

**UNIT III MULTICAST AND TRANSPORT PROTOCOL 9**

Multicast over shared media network, multicast routing and addressing, scaping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP.

**UNIT IV MEDIA - ON – DEMAND 9**

Storage and media servers, voice and video over IP, MPEG over ATM/IP, indexing synchronization of requests, recording and remote control.

**UNIT V APPLICATIONS 9**

MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.

**TOTAL : 45 PERIODS**

**REFERENCES**


1. Jon Crowcroft, Mark Handley, Ian Wakeman. Internetworking Multimedia, Harcourt Asia Pvt.Ltd. Singapore, 1998.
2. B.O. Szuprowicz, Multimedia Networking, McGraw Hill, NewYork. 1995
3. Tay Vaughan, Multimedia making it to work, 4ed,Tata McGrawHill, NewDelhi,2000.

**AP9166 VLSI SIGNAL PROCESSING**

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**UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

**UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

**UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

**UNIT IV SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES 9**

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

**UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9**

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

**TOTAL : 45 PERIODS**

**REFERENCES**


1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004


**CU9122 RF SYSTEM DESIGN**

**L T P C**
**3 0 0 3**

**UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES 9**

CMOS: Introduction to MOSFET Physics – Noise: Thermal, shot, flicker, popcorn noise Transceiver Specifications: Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link Transceiver Architectures: Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures – Transmitter: Direct upconversion, Two step upconversion

**UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9**

S-parameters with Smith chart – Passive IC components - Impedance matching networks Amplifiers: Common Gate, Common Source Amplifiers – OC Time constants in bandwidth estimation and enhancement – High frequency amplifier design Low Noise Amplifiers: Power match and Noise match – Single ended and Differential LNAs – Terminated with Resistors and Source Degeneration LNAs.

**UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9**

Feedback Systems: Stability of feedback systems: Gain and phase margin, Root-locus techniques – Time and Frequency domain considerations – Compensation Power Amplifiers: General model – Class A, AB, B, C, D, E and F amplifiers – Linearisation Techniques – Efficiency boosting techniques – ACPR metric – Design considerations

**UNIT IV PLL AND FREQUENCY SYNTHESIZERS 9**

PLL: Linearised Model – Noise properties – Phase detectors – Loop filters and Charge pumps Frequency Synthesizers: Integer-N frequency synthesizers – Direct Digital Frequency synthesizers

**UNIT V MIXERS AND OSCILLATORS 9**

Mixer: characteristics – Non-linear based mixers: Quadratic mixers – Multiplier based mixers: Single balanced and double balanced mixers – subsampling mixers Oscillators: Describing Functions, Colpitts oscillators – Resonators – Tuned Oscillators – Negative resistance oscillators – Phase noise

**TOTAL : 45 PERIODS**

**TEXT BOOKS**


1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.


**AP9160 SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS**

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**UNIT I CIRCUITS AND HARDWARE MODELING 9**

Design of Microelectronic Circuits - Computer Aided Synthesis and optimization-Combinatorial optimization-Boolean Algebra and Application-Hardware Modeling Languages –Compilation and Behavioral optimization.

**UNIT II ARCHITECTURAL LEVEL SYNTHESIS AND OPTIMIZATION 9**

The Fundamental Architectural synthesis Problems-Area and performance Estimation-Control unit synthesis-synthesis of pipelined circuits.

**UNIT III SCHEDULING ALGORITHMS AND RESOURCE SHARING 9**

Unconstrained Scheduling-ASAP Algorithm-ALAP Scheduling Algorithm- Scheduling with Resource Constraints- Scheduling pipelined circuits-Sharing and binding for Dominated circuits-Area Binding-Concurrent Binding –Module selection problems-Structural testability.

**UNIT IV LOGIC-LEVEL SYNTHESIS AND OPTIMIZATION 9**

Logic optimization Principles-Algorithms and logic Minimization –Encoding problems-Multiple-level optimization of logic networks-Algebraic and Boolean model-Algorithm for delay Evaluation-Rule based logic optimization.

**UNIT V SEQUENTIAL LOGIC OPTIMIZATION 9**

Sequential circuit -State Encoding-Minimization methods-Retiming- Finite state machine-testability for synchronous circuits-Algorithm for library binding- Look-Up table - FPGA-Rule-based library binding.

**TOTAL : 45 PERIODS**

**REFERENCES**


1. Giovanni De Micheli, “Synthesis and optimization of Digital Circuits”, Tata McGraw-Hill, 2003.

2. John Paul Shen, Mikko H. Lipasti, “Modern processor Design”, Tata McGraw Hill, 2003

**AP9161 DATA CONVERTERS**

**L T P C**
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**UNIT I SAMPLE AND HOLD CIRCUITS 9**

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

**UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 9**

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

**UNIT III DIGITAL TO ANALOG CONVERSION 9**

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

**UNIT IV ANALOG TO DIGITAL CONVERSION 9**

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

**UNIT V PRECISION TECHNIQUES 9**

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

**TOTAL : 45 PERIODS**

**REFERENCES**

1. Behzad Razavi, “Principles of data conversion system design”, S.Chand and company ltd, 2000.

**AP9162 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS**

**L T P C**
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**UNIT I MICROPROCESSOR ARCHITECTURE 9**

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

**UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9**

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

**UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9**

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

**UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS 9**

Instruction set addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.

**UNIT V PIC MICROCONTROLLER 9**

CPU Architecture – Instruction set – interrupts- Timers- $I^2C$ Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.

**REFERENCES:**


1. Daniel Tabak , ‘’ Advanced Microprocessors” McGraw Hill.Inc., 1995
2. James L. Antonakos , “ The Pentium Microprocessor ‘’ Pearson Education , 1997.
3. Steve Furber , ‘’ ARM System –On –Chip architecture “Addision Wesley , 2000.
4. Gene .H.Miller .” Micro Computer Engineering ,” Pearson Education , 2003.
5. John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.
6. James L.Antonakos ,” An Introduction to the Intel family of Microprocessors ‘’ Pearson Education 1999.
7. Barry.B.Breg,” The Intel Microprocessors Architecture , Programming and Interfacing “ , PHI,2002.
8. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001. Readings: Web links www.ocw.nit.edu www.arm.com

**AP9163 INTRODUCTION TO MEMS SYSTEM DESIGN**

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**UNIT I INTRODUCTION TO MEMS 9**

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelorometers and Micro fluidics, MEMS materials, Micro fabrication

**UNIT II MECHANICS FOR MEMS DESIGN 9**

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

**UNIT III ELECTRO STATIC DESIGN 9**

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

**UNIT IV CIRCUIT AND SYSTEM ISSUES 9**

Electronic Interfaces, Feed back systems, Noise , Circuit and system issues, Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

**UNIT V INTRODUCTION TO OPTICAL AND RF MEMS 9**

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

**TOTAL : 45 PERIODS**

**TEXT BOOKS:**

1.Stephen Santuria," Microsystems Design", Kluwer publishers, 2000.

**REFERENCES:**

1.Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000
2.Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton,2000.
3.Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

**AP9164 HIGH SPEED SWITCHING**

**L T P C**
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**UNIT I LAN SWITCHING TECHNOLOGY 9**

Switching Concepts, switch forwarding techniques, switch path control, LAN Switching, cut through forwarding, store and forward, virtual LANs.

**UNIT II ATM SWITCHING ARCHITECTURE 9**

Blocking networks - basic - and- enhanced banyan networks, sorting networks - merge sorting, re-arrangable networks - full-and- partial connection networks, non blocking networks - Recursive network construction, comparison of non-blocking network, Switching with deflection routing - shuffle switch, tandem banyan switch.

**UNIT III QUEUES IN ATM SWITCHES 9**

Internal Queueing -Input, output and shared queueing, multiple queueing networks – combined Input, output and shared queueing - performance analysis of Queued switches.

**UNIT IV PACKET SWITCHING ARCHITECTURES 9**

Architectures of Internet Switches and Routers- Bufferless and buffered Crossbar switches, Multi-stage switching, Optical Packet switching; Switching fabric on a chip; Internally buffered Crossbars.

**UNIT V IP SWITCHING 9**

Addressing model, IP Switching types - flow driven and topology driven solutions, IP Over ATM address and next hop resolution, multicasting, IPv6 over ATM.

**TOTAL : 45 PERIODS**

**REFERENCES**


1. Achille Pattavina, “Switching Theory: Architectures and performance in Broadband ATM networks ",John Wiley & Sons Ltd, New York. 1998
2. Elhanany M. Hamdi, “High Performance Packet Switching architectures”, Springer Publications, 2007.
3. Christopher Y Metz, “Switching protocols & Architectures”, McGraw Hill Professional Publishing, NewYork.1998.
4. Rainer Handel, Manfred N Huber, Stefan Schroder, “ATM Networks - Concepts Protocols, Applications”, 3rd Edition, Addison Wesley, New York. 1999.

**AP9165 WIRELESS SENSOR NETWORKS**

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**UNIT I CHARACTERISICS OF WSN 9**

Characteristic requirements for WSN - Challenges for WSNs – WSN vs Adhoc Networks - Sensor node architecture – Commercially available sensor nodes –Imote, IRIS, Mica Mote, EYES nodes, BTnodes, TelosB, Sunspot -Physical layer and transceiver design considerations in WSNs, Energy usage profile, Choice of modulation scheme, Dynamic modulation scaling, Antenna considerations.

**UNIT II MEDIUM ACCESS CONTROL PROTOCOLS 9**

Fundamentals of MAC protocols - Low duty cycle protocols and wakeup concepts - Contention-based protocols - Schedule-based protocols - SMAC - BMAC - Traffic-adaptive medium access protocol (TRAMA) - The IEEE 802.15.4 MAC protocol.

**UNIT III ROUTI NG AND DATA GATHERING PROTOCOLS 9**

Routing Challenges and Design Issues in Wireless Sensor Networks, Flooding and gossiping – Data centric Routing – SPIN – Directed Diffusion – Energy aware routing - Gradient-based routing - Rumor Routing – COUGAR – ACQUIRE – Hierarchical Routing - LEACH, PEGASIS – Location Based Routing – GF, GAF, GEAR, GPSR – Real Time routing Protocols – TEEN, APTEEN, SPEED, RAP **-** Data aggregation - data aggregation operations - Aggregate Queries in Sensor Networks - Aggregation Techniques – TAG, Tiny DB.

**UNIT IV EMBEDDED OPERATING SYSTEMS 9**

Operating Systems for Wireless Sensor Networks – Introduction - Operating System Design Issues - Examples of Operating Systems – TinyOS – Mate – MagnetOS – MANTIS - OSPM - EYES OS – SenOS – EMERALDS – PicOS – Introduction to Tiny OS – NesC – Interfaces and Modules- Configurations and Wiring - Generic Components -Programming in Tiny OS using NesC, Emulator TOSSIM.

**UNIT V APPLICATIONS OF WSN 9**

WSN Applications - Home Control - Building Automation - Industrial Automation - Medical Applications - Reconfigurable Sensor Networks - Highway Monitoring - Military Applications - Civil and Environmental Engineering Applications - Wildfire Instrumentation - Habitat Monitoring - Nanoscopic Sensor Applications – Case Study: IEEE 802.15.4 LR-WPANs Standard - Target detection and tracking - Contour/edge detection - Field sampling.

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. Kazem Sohraby, Daniel Minoli and Taieb Znati, " Wireless Sensor Networks Technology, Protocols, and Applications", John Wiley & Sons, 2007.
2. Holger Karl and Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley & Sons, Ltd, 2005.

3. K. Akkaya and M. Younis, “A survey of routing protocols in wireless sensor networks”, Elsevier Ad Hoc Network Journal, Vol. 3, no. 3, pp. 325--349, 2005.
4. Philip Levis, “ TinyOS Programming”,2006 – www.tinyos.net
5. Anna Ha´c, “Wireless Sensor Network Designs”, John Wiley & Sons Ltd, 2003.
6. Feng Zhao, Leonidas. J.Guibas , “Wireless Sensor Networks” , Morgan Kaufmann Publishers 2000.