UNIVERSITY DEPARTMENTS

ANNA UNIVERSITY CHENNAI : : CHENNAI 600 025

REGULATIONS - 2009

CURRICULUM I TO IV SEMESTERS (FULL TIME)

M.E. VLSI DESIGN

SEMESTER I

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1	MA9109	Applied Mathematics for Electronics Engineers	3	1	0	4
2	AP9112	Digital CMOS VLSI Design	3	0	0	3
3	AP9113	Analog Integrated Circuit Design	3	0	0	3
4	AP9114	Statistical Signal Processing	3	0	0	3
5	VL9111	CAD for VLSI Circuits	3	0	0	3
6	E1	Elective I	3	0	0	3
PRACTICAL						
7	VL9115	VLSI Design Laboratory–I	0	0	4	2
		TOTAL	**18**	**1**	**4**	**21**

SEMESTER II

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1	AP9122	Digital Image Processing	3	0	0	3
2	AP9154	Computer Architecture	3	0	0	3
3	E2	Elective II	3	0	0	3
4	E3	Elective III	3	0	0	3
5	E4	Elective IV	3	0	0	3
6	E5	Elective V	3	0	0	3
PRACTICAL						
7	VL9125	VLSI Design Laboratory- II	0	0	4	2
		TOTAL	**18**	**0**	**4**	**20**

SEMESTER III

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1	E6	Elective VI	3	0	0	3
2	E7	Elective VII	3	0	0	3
3	E8	Elective VIII	3	0	0	3
PRACTICAL						
4	VL9134	Project Work - Phase I	0	0	12	6
		TOTAL	**9**	**0**	**12**	**15**

SEMESTER IV

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
PRACTICAL						
1	VL9141	Project Work – Phase II	0	0	24	12
		TOTAL	**0**	**0**	**24**	**12**

UNIVERSITY DEPARTMENTS

ANNA UNIVERSITY CHENNAI : : CHENNAI 600 025

REGULATIONS - 2009

CURRICULUM I TO VI SEMESTERS (PART TIME)

M.E. VLSI DESIGN

SEMESTER I

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	MA9109	Applied Mathematics for Electronics Engineers	3	1	0	4
2.	AP9112	Digital CMOS VLSI Design	3	0	0	3
3.	AP9113	Analog IC Design	3	0	0	3
		TOTAL	**9**	**1**	**0**	**10**

SEMESTER II

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	AP9154	Computer Architecture	3	0	0	3
2.	E1	Elective I	3	0	0	3
3.	E2	Elective II	3	0	0	3
		TOTAL	**9**	**0**	**0**	**9**

SEMESTER III

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	AP9114	Statistical Signal Processing	3	0	0	3
2.	VL9111	CAD for VLSI Circuits	3	0	0	3
3.	E3	Elective III	3	0	0	3
PRACTICAL						
4.	VL9115	VLSI Design Laboratory –I	0	0	4	2
		TOTAL	**9**	**0**	**4**	**11**

SEMESTER IV

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	AP9122	Digital Image Processing	3	0	0	3
2.	E4	Elective IV	3	0	0	3
3.	E5	Elective V	3	0	0	3
PRACTICAL						
4.	VL9125	VLSI Design Laboratory- II	0	0	4	2
		TOTAL	**9**	**0**	**4**	**11**

SEMESTER V

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	E6	Elective VI	3	0	0	3
2.	E7	Elective VII	3	0	0	3
3.	E8	Elective VIII	3	0	0	3
PRACTICAL						
4.	VL9134	Project Work – Phase I	0	0	12	6
		TOTAL	**9**	**0**	**12**	**15**

SEMESTER VI

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
PRACTICAL						
1.	VL9141	Project Work – Phase II	0	0	24	12
		TOTAL	**0**	**0**	**24**	**12**

LIST OF ELECTIVES

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
1	CP9162	ASIC Design	3	0	0	3
2	AP9152	Hardware Software Co-Design	3	0	0	3
3	VL9151	VLSI Signal Processing.	3	0	0	3
4	VL9152	Testing of VLSI Circuits	3	0	0	3
5	AP9157	Selected Topics in IC Design	3	0	0	3
6	VL9153	Design of Semiconductor Memories	3	0	0	3
7	VL9154	VLSI Technology	3	0	0	3
8	VL9155	Optimization Techniques and their Applications in VLSI Design	3	0	0	3
9	CU9122	RF System design	3	0	0	3
10	AP9153	Signal integrity for high speed design	3	0	0	3
11	AP9161	Data Converters	3	0	0	3
12	VL9156	Solid State Devices Modeling and Simulation	3	0	0	3
13	CP9163	Embedded Systems	3	0	0	3
14	AP9163	Introduction to MEMS System Design	3	0	0	3
15	VL9157	VLSI For Wireless Communications	3	0	0	3

MA9109 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS

L T P C
3 1 0 4

UNIT I FUZZY LOGIC 9

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II MATRIX THEORY 9

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications.

UNIT III ONE DIMENSIONAL RANDOM VARIABLES 9

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV DYNAMIC PROGRAMMING 9

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V QUEUEING MODELS 9

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

L = 45: T=15; TOTAL: 45 PERIODS

REFERENCES:

1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000.
3. Richard Johnson, Miller & Freund. ,Probability and Statistics for Engineers, 7^{th} Edition, Prentice – Hall of India, Private Ltd., New Delhi (2007).
4. Taha, H.A., Operations Research, An introduction, 7^{th} edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, Fundamentals of Queueing theory, 2^{nd} edition, John Wiley and Sons, New York (1985).

AP9112 **DIGITAL CMOS VLSI DESIGN**

L	T	P	C
3	0	0	3

UNIT I MOS TRANSISTOR PRINCIPLES **9**

MOS Technology and VLSI, Process parameters and considerations for, MOS and CMOS, Electrical properties of CMOS circuits and Device modelling. CMOS Inverter Scaling CMOS circuits, Scaling principles and fundamental limits.

UNIT II COMBINATIONAL LOGIC CIRCUITS **9**

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III SEQUENTIAL LOGIC CIRCUITS **9**

Static and Dynamic Latches and Registers, Timing Issues, Pipelines, Clocking strategies, Memory Architectures, and Memory control circuits, Synchronous and Asynchronous Design.

UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS **9**

Datapath circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs

UNIT V IMPLEMENTATION STRATEGIES **9**

Full Custom and Semicustom Design, Standard Cell design and cell libraries, FPGA building block architectures, FPGA interconnect routing procedures, Benchmark Circuits, Case Studies.

TOTAL : 45 PERIODS

REFERENCES

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective". Second Edition, Feb 2003, Prentice Hall of India.
2. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". Second Edition, 1993 Addision Wesley,
3. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
4. Anantha Chandrakasan, W.J, Bowhill and F.Fox, "Design of High Performance Microprocessor Circuits", John Wiley, 2000.

AP9113 ANALOG INTEGRATED CIRCUIT DESIGN

L	T	P	C
3	0	0	3

UNIT I SINGLE STAGE AMPLIFIERS 9

Common source stage, Source follower, Common gate stage, Cascode stage, Single ended and differential operation, Basic differential pair, Differential pair with MOS loads

UNIT II FREQUENCY RESPONSE AND NOISE ANALYSIS 9

Miller effect ,Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascode stage, Differential pair, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III OPERATIONAL AMPLIFIERS 9

Concept of negative feedback, Effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION 9

General considerations, Multipole systems,Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

UNIT V BIASING CIRCUITS 9

Basic current mirrors, cascode current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

TOTAL : 45 PERIODS

REFERENCES:

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 2001
2. Willey M.C. Sansen, “Analog design essentials”, Springer, 2006.
3. Grebene, “Bipolar and MOS Analog Integrated circuit design”, John Wiley & sons,Inc., 2003.
4. Phillip E.Allen, DouglasR.Holberg, “CMOS Analog Circuit Design”, Second edition, Oxford University Press, 2002

AP9114 STATISTICAL SIGNAL PROCESSING

L	T	P	C
3	0	0	3

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9

Discrete Random Processes- Ensemble Averages, Stationary processes, Bias and Estimation, Autocovariance, Autocorrelation, Parseval's theorem, Wiener-Khintchine relation, White noise, Power Spectral Density, Spectral factorization, Filtering Random Processes, Special types of Random Processes – ARMA, AR, MA – Yule-Walker equations.

UNIT II SPECTRAL ESTIMATION 9

Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric methods – ARMA, AR and MA model based spectral estimation, Solution using Levinson-Durbin algorithm

UNIT III LINEAR ESTIMATION AND PREDICTION 9

Linear prediction – Forward and Backward prediction, Solution of Prony's normal equations, Least mean-squared error criterion, Wiener filter for filtering and prediction, FIR and IIR Wiener filters, Discrete Kalman filter

UNIT IV ADAPTIVE FILTERS 9

FIR adaptive filters – adaptive filter based on steepest descent method- Widrow-Hopf LMS algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo cancellation, Adaptive noise cancellation, RLS adaptive algorithm.

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING 9

Mathematical description of change of sampling rate – Interpolation and Decimation, Decimation by an integer factor, Interpolation by an integer factor, Sampling rate conversion by a rational factor, Polyphase filter structures, Multistage implementation of multirate system, Application to subband coding – Wavelet transform

TOTAL : 45 PERIODS

REFERENCES

1. Monson H. Hayes, 'Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc, Singapore, 2002
2. John J. Proakis, Dimitris G. Manolakis, : Digital Signal Processing', Pearson Education, 2002
3. Rafael C. Gonzalez, Richard E. Woods, " Digital Image Processing", Pearson Education Inc.,Second Edition, 2004 (For Wavelet Transform Topic)

VL9111 CAD FOR VLSI CIRCUITS

L	T	P	C
3	0	0	3

UNIT I VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III FLOOR PLANNING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS 9

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL : 45 PERIODS

REFERENCES

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

VL9115 VLSI DESIGN LAB I

L T P C
0 0 4 2

1. Design Entry Using VHDL or Verilog examples for circuit descriptions using HDL languages sequential and concurrent statements.
2. Structural and behavioral descriptions, principles of operation and limitation of HDL simulators. Examples of sequential and combinational logic design and simulation. Test vector generation.
3. Synthesis principles, logical effort, standard cell based design and synthesis, interpretation synthesis scripts, constraint introduction and library preparation and generation.
4. FPGA programming, I/O interfacing, Analog interfacing, Real time application development.
5. SPICE simulations for small size standard cells.
6. SPICE simulations for analog circuit modules - Common source amplifier, source follower, cascode amplifiers, Differential amplifiers, Two stage Operational Amplifiers.

AP9154 COMPUTER ARCHITECTURE

L T P C
3 0 0 3

UNIT I THEORY OF PARALLELISM **9**

Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors andSIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.

UNIT II PARTITIONING AND SCHEDULING **9**

Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

UNIT III HARDWARE TECHNOLOGIES **9**

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory - backplane bus systems, cache memory organisations, shared memory organisations, sequential and weak consistency models.

UNIT IV PIPELINING AND SUPERSCLAR TECHNOLOGIES 9

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V SOFTWARE AND PARALLEL PROGRAMMING 9

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45 PERIODS

REFERENCES:

1. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer architecture – A design Space Approach" , Pearson education , 2003.
2. Kai Hwang, " Advanced Computer Architecture ", McGraw Hill International, 1993.
3. John P.Shen, "Modern processor design - Fundamentals of super scalar processors", Tata McGraw Hill 2003.
4. Kai Hwang, "Scalable parallel computing", Tata McGraw Hill 1998..
5. William Stallings, "Computer Organization and Architecture", Macmillan Publishing Company, 1990.
6. M.J. Quinn, "Designing Efficient Algorithms for Parallel Computers", McGraw Hill International, 1994.

AP9122 DIGITAL IMAGE PROCESSING L T P C
3 0 0 3

UNIT I DIGITAL IMAGE FUNDAMENTALS 9

Elements of digital image processing systems, Vidicon and Digital Camera working principles, Elements of visual perception, brightness, contrast, hue, saturation, Mach Band effect, Image sampling, Quantization, Dither, Two dimensional mathematical preliminaries.

UNIT II IMAGE TRANSFORMS 9

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III IMAGE ENHANCEMENT AND RESTORATION 9

Histogram modification, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contraharmonic and Yp mean filters . Design of 2D FIR filters. Image restoration - degradation model, Unconstrained and Constrained restoration, Inverse filtering-removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations-spatial transformations, Gray Level interpolation. .

UNIT IV IMAGE SEGMENTATION AND RECOGNITION 9

Image segmentation - Edge detection, Edge linking and boundary detection, Region growing, Region splitting and Merging, Image Recognition - Patterns and pattern

classes, Matching by minimum distance classifier, Matching by correlation., Neural networks-Backpropagation network and training, Neural network to recognize shapes.

UNIT V IMAGE COMPRESSION 9

Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding, Transform coding, JPEG standard, JPEG 2000, EZW, SPIHT, MPEG.

TOTAL : 45 PERIODS

REFERENCES

1. Rafael C. Gonzalez, Richard E. Woods, " Digital Image Processing", Pearson Education, Inc., Second Edition, 2004
2. Anil K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall of India, 2002.
3. Rafael C. Gonzalez, Richard E. Woods, Steven Eddins," Digital Image Processing using MATLAB", Pearson Education, Inc., 2004.
4. D.E. Dudgeon and R.M. Mersereau, "Multidimensional Digital Signal Processing", Prentice Hall Professional Technical Reference, 1990.
5. William K. Pratt, " Digital Image Processing", John Wiley, New York, 2002.
6. Milan Sonka et al, "Image Processing, Analysis and Machine Vision", Brookes/Cole, Vikas Publishing House, 2nd edition, 1999;
7. Sid Ahmed, M.A., " Image Processing Theory, Algorithms and Architectures", McGrawHill, 1995.

VL9125 VLSI DESIGN LABORATORY - II

L T P C
0 0 4 2

VLSI based experiments using MAGMA / CADENCE / TANNER / XILINX / ALTERA / ACTEL

1. ASIC RTL realization- MAGMA/CADENCE.
2. Interpretation of standard cell library descriptions, Boolean optimization, optimization for area, power – MAGMA/CADENCE.
3. Static Timing analyses procedures and constraints. Critical path considerations – MAGMA/CADENCE.
4. Scan chain insertion, Floor Planning Routing and Placement procedures and alternatives. Back annotation, layout generation, LVS, Formal verification – MAGMA/CADENCE
5. Layout generation for analog circuit modules- CADENCE/TANNER
6. LVS, Back annotation- CADENCE / TANNER

CP9162 ASIC DESIGN

L T P C
3 0 0 3

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture .

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation - boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL : 45 PERIODS

REFERENCES

1. M.J.S .Smith, " Application - Specific Integrated Circuits ", Addison -Wesley Longman Inc., 1997.
2. Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, “Field Programmable Gate Arrays” Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
6. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

AP9152 HARDWARE / SOFTWARE CO-DESIGN

L	T	P	C
3	0	0	3

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems , Hardware/Software Co-Design , Co-Design for System Specification and Modeling , Co-Design for System Specification and Modelling , Co-Design for Heterogeneous Implementation - Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification .

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, The Hardware/Software Partitioning Problem , Hardware/Software Cost Estimation, Generation of the Partitioning Graph , Formulation of the HW/SW Partitioning Problem , Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms .

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques ,Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification , Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation

TOTAL : 45 PERIODS

REFERENCES

1. Ralf Niemann , “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup , Wayne Wolf ,”Hardware/Software Co-Design: Principles and Practice” , Kluwer Academic Pub,1997.
3. Giovanni De Micheli , Rolf Ernst Morgon,” Reading in Hardware/Software Co-Design “ Kaufmann Publishers,2001.

VL9151 VLSI SIGNAL PROCESSING

L	T	P	C
3	0	0	3

UNIT I INTRODUCTION TO DSP SYSTEMS 9

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II RETIMING 9

Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION 9

Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement.

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS 9

Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL : 45 PERIODS

REFERENCES

1. Keshab K.Parhi, " VLSI Digital Signal Processing systems, Design and implementation ", Wiley, Inter Science, 1999.
2. Gary Yeap, 'Practical Low Power Digital VLSI Design,' Kluwer Academic Publishers, 1998.

3. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw-Hill, 1994.
4. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

VL9152 TESTING OF VLSI CIRCUITS

L	T	P	C
3	0	0	3

UNIT I BASICS OF TESTING AND FAULT MODELLING **9**

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.

UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS **9**

Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY **9**

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches.

UNIT IV SELF-TEST AND TEST ALGORITHMS **9**

Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS **9**

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

TOTAL : 45 PERIODS

REFERENCES:

1. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4. A.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.

AP9157 SELECTED TOPICS IN IC DESIGN

L	T	P	C
3	0	0	3

UNIT I VOLTAGE AND CURRENT REFERENCES **9**

PTAT current references, startup circuits and frequency compensation, CTAT current references, Temperature- independent current references, PTAT current generators, Voltage references, Zero-order references, first order references, Second-order references, state-of-the-Art Curvature-correction techniques.

UNIT II PRECISION REFERENCE CIRCUITS 9

Error source, The output stage, Designing for power supply rejection and line regulation, Effect of resistors temperature coefficient on a reference.

UNIT III OSCILLATOR FUNDAMENTALS 9

General considerations, Ring oscillators, LC oscillators, monolithic inductors, monolithic varactors, Quadrature oscillators, distributed oscillators, voltage controlled oscillators, mathematical model of VCOs.

UNIT IV PHASE LOCK LOOPS 9

Basic PLL topology, Charge-Pump PLLs, nonideal effects in PLLs, Delay locked loops, Frequency multiplication and synthesis, skew reduction, Jitter reduction.

UNIT V CLOCK AND DATA RECOVERY 9

General considerations, Phase detectors for random data, frequency detectors for random data, Full rate referenceless architecture, Dual-VCO Architecture, Dual-loop architecture with external reference, jitter in CDR circuits.

TOTAL : 45 PERIODS

REFERENCES

1. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgap circuits",John wiley & Sons, Inc 2002.
2. Michiel Steyaert , Arthur H. M. van Roermund, Herman Casier "Analog Circuit Design High-
3. speed Clock and Data Recovery, High-performance Amplifiers Power Management " springer, 2008.
4. Behzad Razavi, " Design of Integrated circuits for Optical Communications", Mc Graw Hill, 2003.

VL9153 DESIGN OF SEMICONDUCTOR MEMORIES

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UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES 9

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.

Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.

UNIT II NONVOLATILE MEMORIES 9

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-GateEPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

UNIT III MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE 9

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing

UNIT IV RELIABILITY AND RADIATION EFFECTS 9

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modeling, Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

UNIT V PACKAGING TECHNOLOGIES 9

Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive. Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

TOTAL:45 PERIODS

REFERENCES

a. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice-Hall of India Private Limited, New Delhi, 1997.
b. Tegze P.Haraszti, “CMOS Memory Circuits”, Kluwer Academic publishers, 2001.
c. Betty Prince, “ Emerging Memories: Technologies and Trends”, Kluwer Academic publishers, 2002.

VL9154 VLSI TECHNOLOGY

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UNIT I CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION 9

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II LITHOGRAPHY AND RELATIVE PLASMA ETCHING 9

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments,

UNIT III DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALISATION 9

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION 9

Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

UNIT V ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES 9

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

TOTAL : 45 PERIODS

REFERENCES

1. S.M.Sze, "VLSI Technology", Mc.Graw.Hill Second Edition. 2002.
2. Douglas A. Pucknell and Kamran Eshraghian, " Basic VLSI Design", Prentice Hall India 2003.
3. Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design Prentice Hall India.2000.
4. 4.Wayne Wolf ,"Modern VLSI Design", Prentice Hall India.1998.

VL9155 OPTIMIZATION TECHNIQUES AND THEIR APPLICATIONS IN VLSI DESIGN

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UNIT I STATISTICAL MODELING 9

Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom's model, Principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models

UNIT II STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS 9

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation

UNIT III CONVEX OPTIMIZATION 9

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Max- monomial fitting, Posynomial fitting.

UNIT IV GENETIC ALGORITHM 9

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement,routing technology,Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiway Partitioning Hybrid genetic-encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

UNIT V GA ROUTING PROCEDURES AND POWER ESTIMATION 9

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

TOTAL : 45 PERIODS

REFERENCES

1. Ashish Srivastava, Dennis Sylvester, David Blaauw "Statistical Analysis and Optimization for VLSI:Timing and Power" , Springer, 2005.
2. Pinaki Mazumder, E.Mrudnick, "Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,1998.
3. Stephen Boyd, Lieven Vandenberghe " Convex Optimization", Cambridge University Press, 2004.

CU9122 RF SYSTEM DESIGN

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UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES 9

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT IV PLL AND FREQUENCY SYNTHESIZERS 9

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers

UNIT V MIXERS AND OSCILLATORS 9

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators, Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

TOTAL : 45 PERIODS

TEXT BOOKS

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.

AP9153 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN

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UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stipline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic,Common-mode current, differential-mode current , Connectors

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL =45 PERIODS

REFERENCES

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR , 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.

TOOLS REQUIRED

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

AP9161 DATA CONVERTERS

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UNIT I SAMPLE AND HOLD CIRCUITS 9

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

UNIT II SWITCH CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

UNIT III DIGITAL TO ANALOG CONVERSION 9

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

UNIT IV ANALOG TO DIGITAL CONVERSION 9

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V PRECISION TECHNIQUES 9

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

TOTAL=45 PERIODS

REFERENCES

1. Behzad Razavi, “Principles of data conversion system design”, IEEE press, 1995.
2. Franco Maloberti, “Data Converters”, Springer, 2007.
3. Rudy van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters” Kluwer Acedamic Publishers, Boston, 2003.

VL9156 SOLID STATE DEVICE MODELING AND SIMULATION

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UNIT I MOSFET DEVICE PHYSICS 9

MOSFET capacitor, Basic operation, Basic modeling,Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II NOISE MODELING 9

Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuits

UNIT III BSIMV4 MOSFET MODELING 9

Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, noise model, junction diode models, Layout-dependent parasitics model.

UNIT IV OTHER MOSFET MODELS 9

The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model)

UNIT V MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE 9

Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests

TOTAL:45 PERIODS

REFERENCES

1. Trond Ytterdal, Yuhua Cheng , Tor A. Fjeldly and Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2003.
2. Christian C. Enz, Eric A. Vittoz, “Charge-based MOS Transistor Modeling The EKV model for low-power and RF IC design”, John Wiley & Sons, Ltd, 2006.

CP9163 **EMBEDDED SYSTEMS**

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UNIT I EMBEDDED PROCESSORS 9

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM 9

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture

UNIT III NETWORKS 9

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS 9

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES 9

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL : 45 PERIODS

REFERENCES

1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers.
2. Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia.
3. C. M. Krishna and K. G. Shin, “Real-Time Systems” , McGraw-Hill, 1997
4. Frank Vahid and Tony Givargis, “Embedded System Design: A Unified Hardware/Software Introduction” , John Wiley & Sons.
5. Product literature

AP9163 INTRODUCTION TO MEMS SYSTEM DESIGN

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UNIT I INTRODUCTION TO MEMS 9

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelorometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II MECHANICS FOR MEMS DESIGN 9

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III ELECTRO STATIC DESIGN 9

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV CIRCUIT AND SYSTEM ISSUES 9

Electronic Interfaces, Feed back systems, Noise , Circuit and system issues, Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

UNIT V INTRODUCTION TO OPTICAL AND RF MEMS 9

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

TOTAL : 45 PERIODS

TEXT BOOK

1. 1.Stephen Santuria," Microsystems Design", Kluwer publishers, 2000.

REFERENCES

1. 1.Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000
2. 2.Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton,2000.
3. 3.Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

VL9157 VLSI FOR WIRELESS COMMUNICATION

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UNIT I ANALOG TO DIGITAL CONVERSION 9

Performance metrics for Analog-to-digital converters, sampling, band-pass sampling, quantization, Types of Analog-to-digital converters, Sigma Delta Analog-to-digital converters.

UNIT II CODING THEORY ALGORITHMS AND ARCHITECTURE 9

Convolution codes, trellis diagram, viterbi algorithm, soft input decoding, soft output decoding, Turbo codes, LDPC coding, concatenated convolution codes, weight distribution, Space-Time codes, spatial channels, performance measure, Orthogonal space-time block codes, spatial multiplexing.

UNIT III TRANSCIEVER ARCHITECTURE AND ISSUES 9

Receiver Architectures, Superheterodyne receiver, Image rejection receiver,-Hartley and Weaver, Zero IF receiver, Low IF receiver, Transmitter architecture, Superheterodyne transmitter, Direct up transmitter, Two-step-up transmitter, Transceiever architectures for modern wireless systems, Case study.

UNIT IV OFDM SYSYTEM 9

Principle, propagation characteristics,principle, mathematical model, OFDM baseband signal processing,Receiver design, Automatic gain control and DC offset compensation, codesign of Automatic gain control and timing synchronization, codesign of filtering and timing synchronization, Transmit chain setup.

UNIT V ANALOG IMPAIRMENT AND ISSUES 9

Receiver sensitivity and noise figure, DC offsets, LO leakage, Receiver interferers and intermodulation distortion, Image rejection, Quadrature balance and relation to Image rejection, relation to EVM, Peak to average power ratio , Local oscillator pulling in PLL, effect of phase noise in PLL, Effect of phase noise on OFDM systems, Effect of frequency errors on OFDM systems.

TOTAL :45 PERIODS

REFERENCES

1. Pui-In Mak, Seng-Pan U, Rui Paulo Martins, “Analog-baseband architectures and Circuits for multistandard and low voltageWireless transceivers”, springer, 2007.
2. Emad N. Farag, Mohamed I. Elmasry, “Mixed signal VLSI Wireless design Circuits and systems”, Kluwer Academic Publishers, 2002.
3. Andre Neubauer, Jurgen Freudenberger, Volker Kuhn,” Coding theory, Algorithms, Architectures and Applications”, John Wiley & Sons,2007.
4. Wolfgang Eberle, “Wireless Transceiver Systems Design”,Springer, 2008.