PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):

I. To enrich students to excel in research leading to cutting edge technology in VLSI design and embedded systems and creating competent, innovative, and productive professionals in this field.

II. To provide students with a solid foundation in digital and computer architecture principles leading to VLSI design.

III. To understand the various applications and employ embedded systems to find solutions to them with good scientific and engineering knowledge so as to comprehend, analyze, design, and create novel products and solutions for the real life problems.

IV. To provide students with an academic environment aware of excellence, leadership, ethical conduct, positive attitude, societal responsibilities and the lifelong learning needed for a successful professional career.

V. To inculcate entrepreneurial skills in starting industries applying embedded system technologies.

PROGRAMME OUTCOMES (POs):

On successful completion of the programme,

1. Graduates will be able to apply the knowledge of computing, mathematics, science and electronic engineering for designing VLSI circuits.

2. Graduates will have an ability to identify, formulate, investigate and solve the issues related to the design of VLSI and embedded systems.

3. Graduates will have an ability to design and conduct experiments, perform analysis and interpret the problems of VLSI design and embedded systems.

4. Graduates will be able to demonstrate the design of an embedded system, component or process as per needs and specifications.

5. Graduates will demonstrate an ability to visualize and work on laboratory and multidisciplinary tasks.

6. Graduates will have the skills to use modern engineering tools, softwares and equipments to analyze problems.

7. Graduates will demonstrate knowledge of professional and ethical responsibilities.

8. Graduate will be able to communicate effectively in both verbal and written form.

9. Graduate will show the understanding of the impact of engineering solutions on the society and also will be aware of contemporary issues.

10. Graduate will develop confidence in self education and ability for lifelong learning.
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ANNA UNIVERSITY, CHENNAI
AFFILIATED INSTITUTIONS
M.E. VLSI DESIGN AND EMBEDDED SYSTEMS
REGULATIONS – 2017
CHOICE BASED CREDIT SYSTEM
I – IV SEMESTER CURRICULA AND SYLLABI
SEMESTER - I
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# PROFESSIONAL ELECTIVES (PE)

## ELECTIVE - I

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### EMPLOYABILITY ENHANCEMENT COURSES (EEC)

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OBJECTIVES:
- To encourage students to develop a working knowledge of the central ideas of linear algebra;
- To study and understand the concepts of probability and random variable of the various functions;
- To understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete-time Markov chains;
- To formulate and construct a mathematical model for a linear programming problem in real life situation;
- To introduce the Fourier Transform as an extension of Fourier techniques on periodic functions and to solve partial differential equations.

UNIT I  LINEAR ALGEBRA  12

UNIT II  ONE DIMENSIONAL RANDOM VARIABLES  12

UNIT III RANDOM PROCESSES  12
Classification – Auto correlation - Cross correlation - Stationary random process – Markov process —Markov chain - Poisson process – Gaussian process.

UNIT IV  LINEAR PROGRAMMING  12

UNIT V  FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS  12

TOTAL: 60 PERIODS

COURSE OUTCOMES:
On successful completion of this course, students will be able to
CO1: Classify the random process.
CO2: Formulate and develop a mathematical model for linear programming problem
CO3: Apply the concept of fourier transform to real life situation

REFERENCES:
OBJECTIVES:
- To study and realize various building blocks of digital VLSI circuits in transistor level.
- To design the architectural choices and performance tradeoffs involved and to realize circuits in CMOS technology.
- To introduce the design knowledge about CMOS testing and its implementation strategies.

UNIT I MOS TRANSISTOR PRINCIPLES
MOS Technology and VLSI, Pass transistors, NMOS, CMOS Fabrication process and Electrical properties of CMOS circuits and Device modeling, Characteristics of CMOS inverter, Scaling principles and fundamental limits. Propagation Delays, CMOS inverter scaling, Stick diagram, Layout diagram, Layout rules, Elmore’s constant, Logical Effort.

UNIT II COMBINATIONAL LOGIC CIRCUITS
Static CMOS logic Design, Design techniques to improve the speed, power dissipation of CMOS logic, low power design techniques, Ratioed logic, Pass transistor Logic, Transmission gate logic, CPL, DCVSL, Dynamic CMOS logic, Domino logic, Dual Rail logic, NP CMOS logic and NOR array logic.

UNIT III SEQUENTIAL LOGIC CIRCUITS
Static and Dynamic Latches and Registers, Timing Issues, Pipelines, Clocking strategies, Clock Domain Crossing - Analysis, Strategies and Implementation - Memory Architectures, and Memory control circuits.

UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS
Datapath circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area tradeoffs.

UNIT V CMOS TESTING AND IMPLEMENTATION STRATEGIES
Need for testing - Manufacturing test – Design for testability – Boundary scan, Full Custom and Semicustom Design, FPGA building block architectures, FPGA interconnects.

COURSE OUTCOMES:
After completion of this course:
- Ability to expand their knowledge in designing circuit level implementation to realize and test system based architectures, which include digital, memory, and mixed-signal subsystems.

REFERENCES:
OBJECTIVES:

- To learn about the designing of an embedded system for commercial applications.
- To learn the features, architecture and programming of PIC and ARM microcontrollers.
- To study the interfacing peripherals with microcontrollers.
- To learn about the communication protocols in a Microcomputer system.
- To learn about the fundamentals of real-time operating system in an embedded system.

UNIT I INTRODUCTION TO EMBEDDED SYSTEMS

UNIT II ATMEGA MICROCONTROLLERS
Architecture, Features, Memory and memory map, I/O ports, Timers and CCP Devices, ADC, Interrupts, Instruction format, Addressing Modes, Instruction Set, Programming with MPLAB IDE.

UNIT III 16 BIT MICROCONTROLLER
Introduction to 16 bit Processors, MSP430 - RISC CPU Architecture - Compiler friendly features - Instruction sets - Clock System - Memory Subsystem - Bus Architecture, different families in MSP 430 (2xx,4xx,5xx,6xx) - Key differentiating factors between families.

UNIT IV INTERFACING I/O DEVICES AND COMMUNICATION PROTOCOLS
LED, liquid crystal display, Motor (DC, Servo, Stepper), Relays, Keypad, Keyboard, Touch screen, Sensors (thermocouple, force, displacement), SD card, Infrared connectivity, Serial communication protocols (UART, I2C, SPI, CAN, USB, LIN), Parallel communication protocols (PCI, ISA), Wireless communication networks (Bluetooth, Xbee, Wifi, GSM), Global positioning system receivers, Embedded Systems and the internet.

UNIT V MULTITASKING AND THE REAL-TIME OPERATING SYSTEM
The challenges of multitasking and real-time, Achieving multitasking with sequential programming, RTOS, Scheduling and the scheduler, Developing tasks, Data and resource protection - the semaphore, Examples using Salvo Real-time operating systems.

TOTAL:45 PERIODS

OUTCOMES:
After completion of this course:

- Students will be able to interface peripherals with microcontrollers.
- Students will be able to design an embedded system in real time.
- Students will be able to use the communication protocols in application specific.

REFERENCES:
OBJECTIVES:

- The course will discuss the equivalent circuits and models of MOS circuits.
- To analyze bias circuits using CMOS current mirrors.
- To design and analyze the frequency response of multistage differential amplifiers.
- To discuss the stability and frequency compensation of feedback amplifiers.

UNIT I SINGLE STAGE AMPLIFIERS

Review of MOS physics and equivalent circuits and models. Large and Small signal analysis CS, CG and source follower, miller effect, frequency response of CS, CG and source follower.

UNIT II CURRENT MIRRORS

Current Sources, Basic Current Mirrors, Cascode stages for Current mirrors, Wilson Current Mirror, Large and small signal analysis of current mirrors.

UNIT III MULTISTAGE DIFFERENTIAL AMPLIFIERS

Differential amplifier, Large and small signal analysis of the balanced differential amplifier, device mismatches in differential amplifier, small and large signal analysis of the differential pair with current mirror load, PSRR+, PSRR− and CMRR of differential amplifiers, small signal analysis of telescopic amplifier, two-stage amplifier and folded cascaded amplifier.

UNIT IV FREQUENCY RESPONSE OF MULTISTAGE DIFFERENTIAL AMPLIFIERS

Dominant-Pole approximation, zero-value time constant analysis, - Frequency response of current mirror loaded, differential amplifier, short circuit time constants, frequency response of telescopic cascaded, folded cascode amplifier.

UNIT V STABILITY AND FREQUENCY COMPENSATION OF FEEDBACK AMPLIFIERS

Properties and types of negative feedback circuits, feedback configurations, effect of loading in feedback networks, feedback circuit analysis using return ratio- modelling input and output port in feedback network, the relation between gain and bandwidth in feedback amplifiers, phase margin, frequency compensation, compensation of two stage MOS amplifiers.

TOTAL:45 PERIODS

COURSE OUTCOMES:

After completion of this course, students are expected to:

- Be able to analyze and design CMOS analog IC building blocks like MOS amplifiers, current mirrors and multistage differential amplifiers.

REFERENCES:

OBJECTIVES:

- To introduce methods to analyze and design synchronous and asynchronous sequential circuits.
- To introduce the architectures of programmable devices.
- To introduce design and implementation of digital circuits using programming tools.

UNIT I  SEQUENTIAL CIRCUIT DESIGN  9
Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN  9
Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III  FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS  9

UNIT IV  SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES  9
Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V  SYSTEM DESIGN USING VERILOG  9

TOTAL : 45 PERIODS

COURSE OUTCOMES:
At the end of the course, the student should be able to:

- Analyze and design sequential digital circuits
- Identify the requirements and specifications of the system required for a given application
- Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:

OBJECTIVES:
- To study the basic concepts of digital CMOS Application Specific Integrated Circuit (ASIC) systems design and library cell design.
- To know the architectural details of programmable ASICs.
- To present the ASIC physical design flow, including logic synthesis, floor-planning, placement and routing.
- To know back-end physical design flow steps through VLSI CAD tools.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING
System partitioning - partitioning methods - floor planning - placement - physical design flow – Routing - global routing - detailed routing - special routing - circuit extraction -DRC.

COURSE OUTCOMES:
Upon completion of this course, the students will:
- Be able to design the ASIC implementation using programmable ASIC devices.
- Be able to comprehend the different issues related to the development of ASIC designs including logic synthesis, floor-planning, placement and routing, tools and future trends.

REFERENCES:
OBJECTIVES:
- To understand the various analog and digital circuits and their simulation using Cadence tool.
- To learn the advanced concepts of modern VLSI circuit and system design
- To design common sequential functions: flip-flops, registers, latches, and state-machines.
- To understand placement, routing, and verify timing of a standard cell design.

DIGITAL DESIGN (HDL Design Entry Tool):
1. HDL based design entry and simulation of Parameterizable cores of Counters, Shift registers, State machines, 8-bit Parallel adders and 8 – Bit multipliers.
2. HDL based design entry and simulation of Parameterizable cores on the simple Distributed Arithmetic system.
3. HDL based design entry and simulation of Parameterizable cores on memory design and 4 – bit ALU.
4. Synthesis, P&R and post P&R simulation, Critical paths and static timing analysis results to be identified.

ANALOG IC DESIGN (USING SPICE CIRCUIT SIMULATION TOOL):
Circuit simulation, Layout generation, parasitic extraction, Synthesis and Standard cell based design of the circuits. Identification of critical paths, power consumption. P&R, power and clock routing, post P&R simulation and Static timing analysis of:
1. Design of CMOS Inverter - Circuit Simulation, transfer characteristic curve, transient analysis, Layout design.

TOTAL : 60 PERIODS

COURSE OUTCOMES:
After the completion of this lab, Students should be able:
- To create the hierarchical decomposition of sequential designs.
- To perform synthesis and analysis of combinational and sequential designs.

OBJECTIVE:
FPGAs are important platform used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes, the students will be carrying out complete hardware level FPGA validation of important digital algorithms.

EXPERIMENTS:
1. Design Entry Using VHDL or Verilog using HDL languages of
   i. Combinational circuits namely 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder.
   ii. Sequential circuits namely D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters.
2. Test vector generation and timing analysis of sequential and combinational logic design in (1).
paths to be identified. Identify and verify possible conditions under which the blocks will fail to
work correctly.
4. FPGA implementation of PCI Bus & arbiter.
5. Interfacing with Memory modules in FPGA Boards.
6. Realization of Discrete Fourier transform/Fast Fourier Transform algorithm in HDL
and observing the spectrum in simulation.
7. Verification of design functionality implemented in FPGA by capturing the signal in DSO.
8. Verifying design functionality using either chipscope feature (Xilinx) /the signal tap feature
(Altera)/other equivalent feature. Invoke the PLL and demonstrate the use of the PLL module
for clock generation in FPGAs.

TOTAL : 60 PERIODS

COURSE OUTCOMES:
At the end of the course, the student should be able to
CO1: Write HDL codes for digital circuits satisfying given specification.
CO2: Import the logic modules into FPGA Boards.
CO3: Synthesis, Place and Route the digital IPs.
CO4: Use FPGA EDA tools for design and analysis.

CU5092 REAL TIME EMBEDDED SYSTEMS LT P C
3 0 0 3

OBJECTIVES:
- To study the basic concepts of ARM processors
- To understand the computing platform and design analysis of ARM processors
- To study the concepts of Operating systems in ARM
- To study the concept of embedded networks
- To understand case studies related to embedded systems

UNIT I INTRODUCTION TO ARM PROCESSORS 9
Fundamentals of ARM, ARM Instruction set, Thumb Instruction set, ARM assembly language
programming, Digital Signal Processing in ARM, Exceptions & Interrupt Handling.

UNIT II COMPUTING PLATFORM AND DESIGN ANALYSIS 9
CPU buses – Memory devices – I/O devices – Memory Protection Units – Memory Management
Units – Component interfacing – Design with microprocessors – Development and Debugging –
Program design – Model of programs – Assembly and Linking – Basic compilation techniques –
Analysis and optimization of execution time, power, energy, program size – Program validation
and testing.

UNIT III PROCESS AND OPERATING SYSTEMS 9
Multiple tasks and multi processes – Processes – Context Switching – Scheduling policies -
Multiprocessor – Inter Process Communication mechanisms – Evaluating operating system
performance – Power optimization strategies for processes – Firmware and Operating Systems for
ARM processor.

UNIT IV HARDWARE ACCELERATES & NETWORKS 9
Accelerators – Accelerated system design – Distributed Embedded Architecture – Networks for
Embedded Systems – Network based design – Internet enabled systems.
UNIT V  CASE STUDY  9  
Hardware and software co-design - Data Compressor - Software Modem – Personal Digital Assistants – Set–Top–Box. – System-on-Silicon – FOSS Tools for embedded system development.

COURSE OUTCOMES:  
At the end of this course, the student should be able to:  
- Revise computing platform and design analysis  
- Demonstrate multiple tasks and multi processes  
- Discuss hardware and software co-design  

REFERENCES:  
UNIT V  NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING

COURSE OUTCOME:
- Ability to modify the existing or new DSP architectures suitable for VLSI.

REFERENCES:

VE5201  HARDWARE SOFTWARE CO DESIGN OF EMBEDDED SYSTEM  L  T  P  C
3  0  0  3

OBJECTIVES:
- To introduce the key concepts of hardware/software communication to make trade-offs between the flexibility and the performance of a digital system.
- To learn the concept of integration of custom hardware components with software.
- Students will gain design and implementation experience with case studies.

UNIT I  NATURE OF HARDWARE AND SOFTWARE
Hardware, Software, Definition of Hardware/Software Co-Design – Driving factors Platform design space – Application mapping – Dualism of Hardware design and software design – Concurrency and parallelism, Data flow modeling and Transformation – Data Flow Graph – Tokens, actors and queues, Firing rates, firing rules and Schedules – Synchronous data flow graph – control flow modeling – Adding time and resources – Transformations.

UNIT II  DATA FLOW IMPLEMENTATION IN SOFTWARE AND HARDWARE

UNIT III  DESIGN SPACE OF CUSTOM ARCHITECTURES
Finite state machines with datapath – FSMD design example, Limitations – Microprogrammed Architecture – Microprogrammed control, microinstruction encoding, Microprogrammed data path, microprogrammed machine – General purpose Embedded Core – RISC pipeline, Program organization – SoC interfaces for custom hardware – Design Principles in SoC Architecture

UNIT IV  HARDWARE SOFTWARE INTERFACES
Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling - On-chip buses – Memory mapped interfaces – coprocessor interfaces – custom instruction interfaces – Coprocessor hardware interface – Data and control design, programmer’s model.
UNIT V CASE STUDIES

TOTAL: 45 PERIODS

COURSE OUTCOMES:
On completion of the course, a student should be able:

- To analyze and apply design methodologies.
- To appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their interrelationships.
- To be familiar with modern hardware/software tools for building prototypes and to be able to demonstrate practical competence in these areas

REFERENCES:

VL5202 LOW POWER VLSI DESIGN L T P C
3 0 0 3

OBJECTIVES:
- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

UNIT I POWER DISSIPATION IN CMOS

UNIT II POWER OPTIMIZATION
Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS
Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION
Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic power analysis.
UNIT V SYNTHEISIS AND SOFTWARE DESIGN FOR LOW POWER
Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
- The student will get to know the basics and advanced techniques in low power design which is a hot topic in today’s market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

REFERENCES:

VE5211 EMBEDDED SYSTEMS DESIGN LABORATORY L T P C 0 0 4 2

OBJECTIVES:
- Students have knowledge about the basic functions of embedded systems.
- Students have knowledge in programming skills.

EXPERIMENTS:
ATMEGA / RASPBERRY PI Microcontroller based Experiments with MPLAB IDE from Microchip/
μVision IDE for ARM programming from Keil:
1. Interfacing basic digital input output devices.
2. Interfacing a character LCD.
3. Interfacing A/D and D/A converter.
4. Interfacing Capture/Compare/PWM module
5. Interfacing with USB/WIFI/BLE.
6. DC motor control.
7. Multiplexing seven segment LED displays.
8. Interfacing Stepper motor and temperature sensor.
10. IoT System Design

TOTAL : 60 PERIODS

COURSE OUTCOMES:
- An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, and sustainability.
OBJECTIVES:
- This course will introduce the features, programming and applications of programmable logic devices.
- Provide VLSI system design experience using FSM.
- Discuss the various implementation strategies with FPGA.

UNIT I  PROGRAMMABLE LOGIC
ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series, CPLD, Cypres FLASH 370 Device Technology, Lattice LSI’s Architectures – 3000 Series – Speed Performance and in system programmability.

UNIT II  FPGAS: FIELD PROGRAMMABLE GATE ARRAYS
Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs, Case studies – Xilinx Virtex-6, Spartan-6 FPGAs, ALTERA’s FLEX 8000/10000 FPGAs, NIOS II Embedded Processor, ACTEL’s IGLOO series, ProASIC3 series FPGAs.

UNIT III  FINITE STATE MACHINES (FSM)

UNIT IV  FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN
Architectures centered around non-registered PLDs. State machine design centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. K Application of One – Hot method. System level design – controller, data path and functional partition.

UNIT V  IMPLEMENTING APPLICATIONS WITH FPGAS

TOTAL:45 PERIODS

COURSE OUTCOMES:
After the completion of this course, the students are to:
- Be able to make the system level designs using FSM and analyze the performance with FPGA.

REFERENCES:
OBJECTIVES:
- The student shall develop an overview and deeper insight into the research and development that is underway to meet future needs of flexible processor solution, for energy efficient reconfigurable architectures with high computing performance.

UNIT I   INTRODUCTION  9
Reconfigurable Computing Systems (RCS) – Evolution of reconfigurable systems – Characteristics of RCS - Advantages and issues, Fundamental concepts & Design steps, Domain specific processors, Application specific processors, Classification of reconfigurable architecture - fine, coarse grain & hybrid architectures

UNIT II   PARALLEL AND ADVANCED PROCESSORS  9
Classification of parallel computers, Multiprocessors and multicomputer, SIMD Processing Architectures, CISC & RISC Processors, VLIW Architectures

UNIT III   RECONFIGURABLE ARCHITECTURES  9
FPGA Technology and Architectures – LUT devices and mapping (Look-up Table) ALU design – Placement and partitioning algorithms – Routing algorithms, Spatial Computing Architectures – Systolic Architectures and Algorithms Systolic Structures

UNIT IV   RECONFIGURATION MANAGEMENT  9
Reconfiguration, Configuration Architectures, Managing the Reconfiguration Process, Reducing Configuration Transfer Time

UNIT V   CASE STUDIES OF FPGA APPLICATIONS  9

TOTAL: 45 PERIODS

COURSE OUTCOMES:
Upon successful completion of the course, the student should be able to:
- Analyze the different architecture principles relevant in parallel and reconfigurable systems.
- Compare the tradeoffs that are necessary to meet the area, power and timing criteria of these systems.
- In depth analysis of current research projects to get broader context and assess its significance.
- Describe and relate new architectures and applications in relations to the previously existing solutions.

REFERENCES:
OBJECTIVES:
- To provide the fundamental concepts of noise in IC, OTA design, switched-capacitor circuits and data conversion circuits.

UNIT I  NOISE IN INTEGRATED CIRCUITS  9
Statistical Characteristics of Noise, Sources of noise, noise models of IC components, Circuit noise calculations, equivalent input noise generators, effect of feedback on noise performance, noise in CS, CE, CG and cascode amplifiers, noise in differential pair, noise bandwidth.

UNIT II  OTA DESIGN CONSIDERATION  9
Step response, Slewing, OTA variations, CMFB implementation, Input resistance, Output resistance, Output Voltage swing, CMRR, PSRR of two-stage telescopic amplifiers.

UNIT III  BANDGAP REFERENCE CIRCUIT AND SWITCHED CAPACITOR CIRCUITS  9

UNIT IV  PERFORMANCE METERICS OF DATA CONVERTERS & NYQUIST RATE D/A CONVERTERS  9
Ideal Sampling, Reconstruction, Quantization, Static performance metrics, Dynamic performance metrics, Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs.

UNIT V  ANALOG TO DIGITAL CONVERTERS  9
Single stage amplifier as comparator, resistor-based latched comparators, offset cancellation, Flash ADC, Successive approximation ADC, Pipelined ADC, Time Interleaved ADC.

COURSE OUTCOMES:
At the completion of the subject, students should:
- Be able to grasp the fundamental concept of noise in IC.
- Be able to study and analyze switched-capacitor circuits and the issue of non-linearity and mismatch in the circuits.
- Be able to analyze data conversion circuits such as DAC and ADC and their design techniques.

REFERENCES:
OBJECTIVES:
- To expose the students to the fundamentals of Network communication technologies.
- To teach the fundamentals of Internet
- To study on Java based Networking
- To introduce network routing Agents
- To study the basis for network on-chip technologies

UNIT I THE HARDWARE INFRASTRUCTURE

UNIT II INTERNET CONCEPTS
Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT III DISTRIBUTED COMPUTING USING JAVA

UNIT IV EMBEDDED AGENT

UNIT V EMBEDDED COMPUTING ARCHITECTURE

TOTAL : 45 PERIODS

COURSE OUTCOMES:
At the completion of the course, students will be able to:
- Explain the fundamentals of Network communication technologies, internet, and Java based networking.
- Analyze the analog/digital co-design of distributed embedded computing architecture.

REFERENCES:
VE5005 COMPUTER AIDED DESIGN FOR VLSI CIRCUITS

OBJECTIVES:
- To discuss the Algorithmic Graph Theory and computational complexity optimization.
- To discuss the concepts of layout design rules and floor planning.
- To simulate and synthesis different hardware models.

UNIT I VLSI DESIGN METHODOLOGIES

UNIT II DESIGN RULES

UNIT III FLOOR PLANNING
Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION
Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis - Circuit and AMS Co-Simulation techniques.

UNIT V MODELLING AND SYNTHESIS

TOTAL : 45 PERIODS

COURSE OUTCOMES:
At the completion of this subject,
- Students will be able to implement, simulate and synthesis the computer aided design of VLSI systems.

REFERENCES:

VE5006 DIGITAL IMAGE AND VIDEO PROCESSING

OBJECTIVES:
- To provide the basic concepts of image & pattern recognition.
- To give an exposure to basic image processing and modeling techniques.
- To provide an understanding of various concepts related to video object extraction.
- To prepare students for development and implementation of algorithms.

UNIT I IMAGE FUNDAMENTALS AND TRANSFORMS
Image Representation- Sampling and Quantization - Two dimensional DFT- Discrete cosine Transform - Walsh - Hadamard transform - Wavelet transform - Construction of Wavelets-Types of wavelets - principal component analysis.
UNIT II PROCESSING AND MODELING OF IMAGES
9
Pre-processing - Point operations – contrast stretching – Histogram - Histogram equalization - Image segmentation- pixel based, edge based, region based segmentation - Morphological image processing - Edge and texture models - Image registration - Colour Image Processing -

UNIT III SPATIAL FEATURE EXTRACTION
9
Feature selection - Localized feature extraction- Boundary Descriptors - Moments - Texture Descriptors - Co-occurrence features

UNIT IV CLASSIFIERS
9
Kernel based approaches - clustering methods - Maximum Likelihood Estimation- Bayesian approach - Pattern Classification

UNIT V VIDEO OBJECT EXTRACTION
9
Back ground subtraction – Frame difference - Static and dynamic background modeling - optical flow techniques-Handling occlusion- scale and appearance changes - Shadow removal.

TOTAL :45 PERIODS

COURSE OUTCOMES:
• To be able to design pattern recognition systems.
• To design and implement feature extraction techniques for a given application.
• To design a suitable classifier for a given application.

REFERENCES:

VE5007 ALGORITHMS FOR VLSI DESIGN AUTOMATION
L  T   P   C
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OBJECTIVES:
• To discuss the algorithms for logic synthesis, verification.
• To discuss about the design tradeoff in various partitioning algorithms, placement, floor planning and pin assignment of VLSI design automation.
• To analyze the different global routing algorithms and compaction in design automation.

UNIT I LOGIC SYNTHESIS & VERIFICATION:
Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis, Introduction to Circuit Simulation - Co - Simulation.

UNIT II PARTITIONING:
Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.
UNIT III  
PLACEMENT, FLOOR PLANNING & PIN ASSIGNMENT:  9
Problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

UNIT IV  
GLOBAL ROUTING:  12
Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization.

UNIT V  
COMPACTIO
N:  9
Problem formulation, one-dimensional compaction, two dimensions based compaction, hierarchical compaction.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
Ability to analyze the algorithms needed for synthesis, partitioning, placement, floor planning, routing in VLSI design automation

REFERENCES:

VE5008  
ADVANCED EMBEDDED SYSTEM DESIGN  L  T  P  C
3  0  0  3

OBJECTIVES
• To teach the fundamentals on design attributes of functional units of embedded systems.
• To discuss about Hardware, software partitioning in system design
• To introduce architectural features of 32 bit ARM microcontroller.
• To discuss strategies for embedded firmware design and development.
• To develop an integrated development environment in embedded system

UNIT I  
TYPICAL EMBEDDED SYSTEM  9

UNIT II  
EMBEDDED HARDWARE DESIGN AND DEVELOPMENT  9
EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction, creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement.
UNIT III   ARM -32 BIT MICROCONTROLLER FAMILY

UNIT IV    EMBEDDED Firmware Design And Development
Embedded Firmware Design Approaches, Embedded Firmware Development Languages, Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

UNIT V     EMBEDDED SYSTEM DEVELOPMENT ENVIRONMENT
The Integrated Development Environment (IDE), Types of Files Generated on Cross compilation, Disassembler/ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan - Hardware Security, Software Security.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
- Ability to discuss the concepts of typical embedded systems.
- Ability to develop an integrated development environment of hardware/software codesign of embedded system.

REFERENCES:

VE5009    POWER MANAGEMENT AND CLOCK DISTRIBUTION CIRCUITS

OBJECTIVES:
- To teach the design of reference circuits and low drop out regulators for desired specifications
- To teach oscillator choice and requirements for clock generation circuits
- To teach the design of clock generation and recovery in the context of high speed systems

UNIT I    VOLTAGE AND CURRENT REFERENCES
Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference, Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II   LOW DROP OUT REGULATORS
UNIT III  OSCILLATOR FUNDAMENTALS
General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for LC & Ring Oscillators, Phase Noise in Differential LC Oscillators.

UNIT IV  CLOCK DISTRIBUTION CIRCUITS

UNIT V  CLOCK AND DATA RECOVERY CIRCUITS
CDR Architectures, Trans Impedance Amplifiers and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Design Band gap reference circuits and Low Drop Out regulator for a given specification.
CO2: Understand specification related to Supply and Clock generation circuits of ICs
CO3: Choose oscillator topology and design meeting the requirement of clock generation circuits.
CO4: Design clock generation circuits in the context of high speed I/Os, High speed Broad Band Communication circuits and Data Conversion Circuits.

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VE5010  ADAPTIVE SIGNAL PROCESSING

OBJECTIVES:
- To provide an in-depth coverage of the adaptive filter theory.
- To provide the mathematical framework for the understanding of adaptive statistical signal processing.
- To know the basic tools of vector spaces and discrete-time stochastic process.
- To understand the various issues involved in adaptive filtering.
- Various types of adaptive filters will be introduced and their properties will be studied, specifically convergence, tracking, robustness and computational complexity.
- Learn to apply adaptive filter theory using prescribed case studies.

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UNIT I  STOCHASTIC PROCESSES AND SPECTRUM ESTIMATION  9

UNIT II  WIENER FILTERS  9

UNIT III  GRADIENT-BASED ADAPTIVE FILTERS  9

UNIT IV  KALMAN FILTERS & TRACKING  9

UNIT V  APPLICATIONS  9

TOTAL: 45 PERIODS

COURSE OUTCOMES:
- To be able to solve the problems related to optimal design, convergence, and recursiveness.
- To carry out time/frequency domain implementations of adaptive filters.
- To be able to apply the concepts of stochastic processes to adaptive filters.
- To be able to design adaptive filter algorithms.
- To be able to apply adaptive filter theory to applications such as echo cancelation, noise cancellation and channel equalization.

REFERENCES:
VE5011 DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES  

OBJECTIVES:
- To understand the architecture and programming of fixed and floating point DSP processors.
- To understand the techniques involved in real time DSP system design and to design and implement a variety of DSP algorithms for real world applications.
- To gain the practical knowledge of real time implementation issues.
- Learn the basic forms of FIR and IIR filters, and design filters with desired frequency responses.
- Understand the fast implementation schemes of DFT.
- Learn to apply adaptive filter theory and implement it in DSP Processor.

UNIT I  INTRODUCTION TO DIGITAL SIGNAL PROCESSING SYSTEMS  9
Fundamentals of DSP - Digital signal processor architectures – Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.

UNIT II  FIXED AND FLOATING POINT DIGITAL SIGNAL PROCESSORS  9
TMS320C55x – Architecture overview, Addressing modes, Instruction set, Programming considerations, system issues. TMS320C62x AND TMS320C64x - Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Realtime implementations.

UNIT III  FAST FOURIER TRANSFORMS  9
Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

UNIT IV  FIR AND IIR FILTER IMPLEMENTATIONS  9
FIR and IIR filters – Characteristics, Structures, FIR Filter design using Windowing and frequency sampling method, IIR Filter-Butterworth and Chebyshev Filter Design-, Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

UNIT V  ADAPTIVE FILTER STRUCTURES AND ALGORITHMS  9
Wiener filter, LS filter , Filter structures, Adaptive algorithms, Properties and Applications – Fixed and floating point implementation using TMS320C64x and TMS320C67x.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
- To be able to develop the program for fixed and floating point DSP processors based on the design issues.
- To be able to design and develop real time implementations on DSP algorithms.
- Ability to design IIR and FIR filters.
- To apply the fast transforms for the analysis of DSP systems.
- To be able to realize and implement a suitable structure for FIR and IIR Filters.
- To be able to design adaptive filter algorithms.

REFERENCES:
5. TMS Manual on TMS320C64XX and TMS320C67XX.
CU5073 VLSI FOR WIRELESS COMMUNICATION

OBJECTIVES:
- To understand the concepts of basic wireless communication concepts.
- To study the parameters in receiver and low noise amplifier design.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of transmitters and power amplifiers in wireless communication.

UNIT I COMMUNICATION CONCEPTS

UNIT II RECEIVER ARCHITECTURE & LOW NOISE AMPLIFIERS
Receiver front end – Filter design – Non-idealities – Design parameters – Noise figure & Input intercept point. LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedance matching & Core amplifier.

UNIT III MIXERS

UNIT IV FREQUENCY SYNTHESIZERS
PLL – Phase detector – Dividers – Voltage Controlled Oscillators – LC oscillators – Ring Oscillators – Phase noise – Loop filters & design approaches – A complete synthesizer design example (DECT) – Frequency synthesizer with fractional divider.

UNIT V TRANSMITTER ARCHITECTURES & POWER AMPLIFIERS
Transmitter back end design – Quadrature LO generator – Power amplifier design.

TOTAL : 45 PERIODS

OUTCOMES:
At the end of this course, the student should be able to
- Design LNA and Mixers
- Evaluate frequency synthesizers
- Design and analyze power amplifiers
REFERENCES:

VE5012 COMPUTATIONAL INTELLIGENCE

OBJECTIVES:
- To understand the fundamentals of computational intelligence
- To know about the various knowledge representation methods
- To understand the features of neural network and its implementation
- To study about various data clustering methods
- To gain knowledge in evolutionary computation and neuro – fuzzy systems

UNIT I INTRODUCTION TO COMPUTATIONAL INTELLIGENCE

UNIT II KNOWLEDGE REPRESENTATION METHODS

UNIT III NEURAL NETWORKS AND LEARNING ALGORITHMS

UNIT IV DATA CLUSTERING METHODS AND ALGORITHMS
A simple project using any one of the above domains with tools like MATLAB, Python 2 and Weka tool 3.7.

TOTAL : 45 PERIODS

COURSE OUTCOMES:
- Implement computational intelligence through applications
- Understand knowledge representation methods and apply approximate reasoning
- Apply evolutionary algorithm to solve the optimization problem
- Gain research Knowledge to develop applications using hybrid systems
- Able to Model Flexible Fuzzy Inference systems for dynamic nonlinear data sets

REFERENCES:
2. Andries Engelbrecht, Computational Intelligence: An Introduction, 2007
VE5013 EMBEDDED C

OBJECTIVES:
- To understand the basics of embedded C programming and its compilers and simulators.
- Apply to C programming in embedded systems.

UNIT I BASICS OF EMBEDDED C
System programming Vs Application Programming-General rules in C, Comments, White Spaces, Modules, Data type, Procedures, Variables, Expression and Statements, Structures and Union, Data structures, Program Description Language.

UNIT II PROGRAMMING
Adding Structure to the Code Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Examples.

UNIT III COMPLIERS AND SIMULATORS
Introduction to MikroC compiler and debugger, Functions and Inbuilt libraries in MikroC, Creating new libraries, Development Tools, Introduction to simulators such as Proteus and Real PIC.

UNIT IV EMBEDDED MEMORY
Mixing Assembly and C, Memory Alignment with Structures, Memory management in C, Memory-map of Applications.

UNIT V CASE STUDIES
Chasing LEDs, LED Dice, Seven Segment LED Counter, Two-Digit Multiplexed Seven Segment LED Counter with Timer Interrupt, Real Time Clock, Digital Voltmeter with LCD, Calculator with Keypad and LCD, Serial Communication Based Calculator, Multitasking and Real-Time Operating Systems.

COURSE OUTCOMES:
- This subject enables our students to create, develop, apply, and disseminate the programming knowledge within the embedded systems development environment.

REFERENCES:

VE5014 DESIGN OF EMBEDDED CONTROL SYSTEM

OBJECTIVES:
- To expose the students to the fundamentals of Embedded System Blocks
- To teach the fundamental RTOS.
- To study on interfacing for processor communication
- To compare types and Functionalities in commercial software tools
- To discuss the Applications development using interfacing
UNIT I  EMBEDDED SYSTEM ORGANIZATION 9
Embedded computing, Characteristics of embedded computing applications, Embedded system design challenges, Build process of Realtime Embedded system, Selection of processor, Memory, I/O devices, Rs-485, MODEM, Bus Communication system using I2C, CAN, USB buses, 8 bit – ISA, EISA bus.

UNIT II  REAL-TIME OPERATING SYSTEM 9
Introduction to RTOS, RTOS- Inter Process communication, Interrupt driven Input and Output, Nonmaskable interrupt, Software interrupt, Thread – Single, Multithread concept, Multitasking Semaphores.

UNIT III  INTERFACE WITH COMMUNICATION PROTOCOL 9
Design methodologies and tools – Design flows – Designing hardware and software Interface, System Integration; SPI, High speed data acquisition and interface, SPI read/write protocol, RTC interfacing and programming.

UNIT IV  DESIGN OF SOFTWARE FOR EMBEDDED CONTROL 9

UNIT V  CASE STUDIES WITH EMBEDDED CONTROLLER 9
Programmable interface with A/D & D/A interface, Digital voltmeter, Control- Robot system, PWM motor speed controller, Serial communication interface.

TOTAL : 45 PERIODS

COURSE OUTCOME:
- Students will be able to realize a real time embedded system.

REFERENCES:

VL5002  RF IC DESIGN  L T P C
3 0 0 3

OBJECTIVES:
- To study the various impedance matching techniques used in RF circuit design.
- To understand the functional design aspects of LNAs, Mixers, PLLs and VCO.
- To understand frequency synthesis.

UNIT I  IMPEDANCE MATCHING IN AMPLIFIERS 9
UNIT II  AMPLIFIER DESIGN  9
Noise characteristics of MOS devices, Design of CG LNA and inductor degenerated LNAs. Principles of RF Power Amplifiers design,

UNIT III  ACTIVE AND PASSIVE MIXERS  9

UNIT IV  OSCILLATORS  9
LC Oscillators, Voltage Controlled Oscillators, Ring oscillators, Delay Cells, tuning range in ring oscillators, Tuning in LC oscillators, Tuning sensitivity, Phase Noise in oscillators, sources of phase noise

UNIT V  PLL AND FREQUENCY SYNTHESIZERS  9
Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase noise in PLL, Loop Bandwidth, Basic Integer-N frequency synthesizer, Basic Fractional-N frequency synthesizer

TOTAL: 45 PERIODS

COURSE OUTCOMES:
To understand the principles of operation of an RF receiver front end and be able to design and apply constraints for LNAs, Mixers and Frequency synthesizers.

REFERENCES:

VE5015  MEMS AND MICROSYSTEMS  L T P C
3 0 0 3

OBJECTIVES:
- To understand the fundamentals of MEMS and Microsystems.
- To learn MEMS accelerometers and actuators design techniques, including interfacing and packaging techniques.

UNIT I  INTRODUCTION TO MEMS  9
MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II  MICROMECHANICS  9
Elasticity, Stress, strain and material properties, Bending of thin films, Spring configurations, torsion deflection, Mechanical vibration, Resonance, Thermomechanics - actuators, force and response time, Fracture and thin film mechanics.
UNIT III MICROACTUATORS 9
Electrostatics: basic theory, electrostatic instability. Surface tension, Gap and finger pull up, Electrostatic actuators, comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators, bistable actuators.

UNIT IV INTERFACING AND PACKAGING 9
Electronic Interfaces, Feedback systems, Noise, Packaging: Dicing-Wafer level Packaging-Wafer bonding-Connections between layers-self assembly-higher level of packaging.

UNIT V CASE STUDIES 9
Optical MEMS, RF MEMS- System design basics, Case studies: Capacitive accelerometer, Peizo electric pressure sensor, MEMS scanners, Capacitive RF MEMS switch, performance issues.

COURSE OUTCOMES:
Upon completion of the course, students will have:
- An ability to analyze the working of MEMS and Microsystems components.
- An ability to design the MEMS accelerometer and to design Electrostatic actuators.
- An ability to analyze the working of RF and Optical MEMS.

REFERENCES:

VE5016 MULTICORE ARCHITECTURES AND PROGRAMMING L T P C 3 0 0 3
OBJECTIVES:
- To discuss the principles of different multiprocessors with their performance issues.
- To discuss the fundamentals of various programming concepts used in multicore architectures.

UNIT I INTRODUCTION TO MULTIPROCESSORS AND SCALABILITY ISSUES 9

UNIT II PARALLEL PROGRAMMING 9

UNIT III OPENMP PROGRAMMING 9
UNIT IV  
MPI PROGRAMMING  
9
MPI Model – collective communication – data decomposition – communicators and topologies – point-to-point communication – MPI Library.

UNIT V  
MULTICORE ARCHITECTURES FOR EMBEDDED SYSTEMS  
9

TOTAL : 45 PERIODS

OUTCOMES:
- Students will be able to explain the principle and operation of multicore architectures and their programming.
- Students will be able to design a multicore architecture for an embedded system.

REFERENCES:
2. Michael J Quinn, Parallel programming in C with MPI and OpenMP, Tata Mcgraw Hill, 2003.

VE5017  
EMBEDDED AUTOMOTIVE SYSTEMS  
L T P C  
3 0 0 3
OBJECTIVES
- To teach the Fundamentals of Electronic Components related to automotive applications.
- To discuss on Automotive Sensors, Actuators and Instrumentations
- To teach the Control Mechanisms in an Automotive System
- To discuss on Telematics and Diagnostic methods

UNIT I  
SYSTEMS APPROACH TO CONTROL AND INSTRUMENTATION  
9

UNIT II  
FUNDAMENTALS OF ELECTRONICS, MICROCOMPUTER INSTRUMENTATION AND CONTROL  
9
Semiconductor Devices, Transistors, ICs, Operational Amplifiers, Use of Feedback in Op Amps, Phase-Locked Loop, Digital Circuits, Logic Circuits (Combination and Sequential Circuits), Timers and Counters, Microcomputer fundamentals, Tasks and Operations, CPU Registers, Reading Instructions, Programming Languages, Microcomputer Hardware, Microcomputer Applications in Automotive Systems, Instrumentation Applications of Mirocomputers, Microcomputers in Control Systems.
UNIT III SENSORS, ACTUATORS AND ELECTRONIC ENGINE CONTROL 9

UNIT IV MOTION AND DIGITAL POWERTRAIN CONTROL SYSTEM 9

UNIT V AUTOMOTIVE INSTRUMENTATION, TELEMATICS AND ITS DIAGNOSTICS 9

TOTAL : 45 PERIODS

OUTCOMES:
At the successful completion of this course, students will be able to:
- Discuss embedded controls and mechanisms involved in an automotive systems

REFERENCES:

VE5018 SoC DESIGN FOR EMBEDDED SYSTEM

OBJECTIVES:
- To introduce architecture and design concepts underlying system on chips.
- Students can gain knowledge of designing SoCs.
- To impart knowledge about the hardware-software design of a modest complexity chip all the way from specifications, modeling, synthesis and physical design.

UNIT I SYSTEM ARCHITECTURE: OVERVIEW
Components of the system – Processor architectures – Memory and addressing – system level interconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.
UNIT II       PROCESSOR SELECTION FOR SOC  9

UNIT III       MEMORY DESIGN  9

UNIT IV       INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION  9

UNIT V       FPGA BASED EMBEDDED PROCESSOR  9

OUTCOMES:
Upon successful completion of the program the students shall

• Explain all important components of a System-on-Chip and an embedded system, i.e. digital hardware and embedded software;
• Outline the major design flows for digital hardware and embedded software;
• Discuss the major architectures and trade-offs concerning performance, cost and power consumption of single chip and embedded systems;

REFERENCES:

TOTAL: 45 PERIODS

VL5005       NETWORKS ON CHIP  L T P C
3 0 0 3

OBJECTIVES:
The students should be made to:

• Understand the concept of network - on - chip
• Learn router architecture designs
• Study fault tolerance network - on – chip

UNIT I       INTRODUCTION TO NOC  9
Introduction to NoC – OSI layer rules in NoC - Interconnection Networks in Network-on-ChipNetwork Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support
UNIT II  ARCHITECTURE DESIGN  9

UNIT III  ROUTING ALGORITHM  9
Packet routing-Qos, congestion control and flow control – router design – network link design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing for 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms

UNIT IV  TEST AND FAULT TOLERANCE OF NOC  9
Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on-Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on-Chips.

UNIT V  THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP  9

TOTAL: 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:

- Compare different architecture design
- Discuss different routing algorithms
- Explain three dimensional networks - on-chip architectures

REFERENCES:

AP5071  NANOELECTRONICS  L T P C
3 0 0 3

OBJECTIVES
- To understand how transistor as Nano device
- To understand various forms of Nano Devices
- To understand the Nano Sensors

UNIT I  SEMICONDUCTOR NANO DEVICES  9
Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single-Electron Transistors; Nanorobotics and Nanomanipulation; Mechanical Molecular Nanodevices; Nanocomputers: Optical Fibers for Nanodevices; Photochemical Molecular Devices; DNA-Based Nanodevices; Gas-Based Nanodevices.
UNIT II  ELECTRONIC AND PHOTONIC MOLECULAR MATERIALS  9

UNIT III  THERMAL SENSORS  9
Thermal energy sensors -temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.

UNIT IV  GAS SENSOR MATERIALS  9
Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity; Discussion of sensors for various gases, Gas sensors based on semiconductor devices.

UNIT V  BIOSENSORS  9
Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential.

TOTAL: 45 PERIODS

OUTCOMES:
• To be able to simulate and design the nano device
• To be able to simulate and design the nano sensors

REFERENCES:

VL5009  DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS  L T P C
3 0 0 3

OBJECTIVES:
• To discuss the algorithmic complexity parameters and the basic algorithmic design techniques.
• To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms and NP Hard Problems.

UNIT I  INTRODUCTION  9
Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II  DESIGN TECHNIQUES  9
Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III  SEARCHING AND SORTING  9
Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior
UNIT IV  GRAPH ALGORITHMS  9
Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm.

UNIT V  SELECTED TOPICS  9

TOTAL: 45 PERIODS

COURSE OUTCOMES:
- Will be able to apply the suitable algorithm according to the given optimization problem.
- Ability to modify the algorithms to refine the complexity parameters.

REFERENCES:

AP5093  ROBOTICS  3 0 0 0 3

OBJECTIVES:
- To understand robot locomotion and mobile robot kinematics
- To understand perception in robotics
- To understand mobile robot localization
- To understand mobile robot mapping
- To understand simultaneous localization and mapping (SLAM)
- To understand robot planning and navigation

UNIT I  LOCOMOTION AND KINEMATICS  9

UNIT II  ROBOT PERCEPTION  9

UNIT III  MOBILE ROBOT LOCALIZATION  9

UNIT IV  MOBILE ROBOT MAPPING  9
UNIT V  PLANNING AND NAVIGATION  9
Introduction to planning and navigation – planning and reacting – path planning – obstacle avoidance techniques – navigation architectures – basic exploration algorithms

TOTAL 45 PERIODS

COURSE OUTCOMES:
Upon Completion of the course, the students will be able to
- Explain robot locomotion
- Apply kinematics models and constraints
- Implement vision algorithms for robotics
- Implement robot localization techniques
- Implement robot mapping techniques
- Implement SLAM algorithms
- Explain planning and navigation in robotics

REFERENCES:

VE5019  EMBEDDED NETWORKING  L T P C  3 0 0 3

OBJECTIVES:
To impart knowledge on
- Serial and parallel communication protocols
- Application Development using USB and CAN bus for PIC microcontrollers
- Application development using Embedded Ethernet.
- Wireless sensor network communication protocols.

UNIT I  COMMUNICATION PROTOCOLS:  9

UNIT II  USB AND CAN BUS:  9

UNIT III  ETHERNET BASICS:  9
UNIT IV  EMBEDDED ETHERNET: 9

UNIT V  WIRELESS EMBEDDED NETWORKING: 9

TOTAL : 45 PERIODS

OUTCOMES:
- Complete knowledge of wired and wireless network protocols
- Should be able to incorporate networks in embedded systems

REFERENCES: