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OBJECTIVES:
Analog circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology. The most important building blocks of all CMOS analog ICs will be the topic of study in this course. The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course. The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.

UNIT I            SINGLE STAGE AMPLIFIERS  12
Basic MOS physics and equivalent circuits and models, CS,, CG and Source Follower cascode and folded cascade configurations, differential amplifiers and current mirror configurations.

UNIT II         HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS  9

UNIT III        FEEDBACK AND OPERATIONAL AMPLIFIERS  9
Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV         STABILITY AND FREQUENCY COMPENSATION  9
General considerations, Multipole systems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

UNIT V          BANDGAP REFERENCES  6
supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

TOTAL : 45 PERIODS

REFERENCES:

OUTCOMES:
• Ability to carry out the design of single and two stage operational amplifiers and voltage references, and determine the device dimensions of each MOSFETs involved.
AP8154  STATISTICAL SIGNAL PROCESSING  L T P C  3 0 0 3

OBJECTIVES:
- To introduce the basics of random signal processing
- Conceptwise introduction to estimation and prediction theory
- To know about adaptive filtering and it’s applications
- A brief overview of the processing of speech signals

UNIT I  INTRODUCTION TO RANDOM SIGNAL PROCESSING  9

UNIT II  SPECTRAL ESTIMATION  9
Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric method, AR (p) spectral estimation and detection of Harmonic signals, MUSIC algorithm.

UNIT III  LINEAR ESTIMATION AND PREDICTION  9
Linear Prediction of Signals-Forward and Backward Predictions, Solution to Prony’s normal equation, Levinson Durbin Algorithm, Lattice filter realization of prediction error filters. Linear Minimum Mean-Square Error (LMMSE) Filtering: Wiener Hopf Equation, FIR Wiener filter, Noise Cancellation, Causal IIR Wiener filter, Noncausal IIR Wiener filter, Discrete Kalman filter

UNIT IV  ADAPTIVE FILTERS  9

UNIT V  APPLICATION OVERVIEW- SPEECH PROCESSING  9
Speech Fundamentals: Articulatory Phonetics – Production and Classification of Speech Sounds; Acoustic Phonetics – acoustics of speech production; Short-term Fourier transform (STFT): overview of Fourier representation, non-stationary signals, development of STFT, transform and filter-bank views of STFT; Short time Homomorphic Filtering of Speech; Linear Prediction (LP) analysis: Basis and development, Levinson-Durbin’s method, normalized error, LPC spectrum.

TOTAL: 45 PERIODS

REFERENCES:

OUTCOMES:
- Well equipped with the concepts of random signal processing
- Prediction and Estimation concepts are well understood
- Aware of adaptive filters and their applications
- Gather basic knowledge about speech signal processing
OBJECTIVES:
- To encourage students to develop a working knowledge of the central ideas of linear algebra;
- To study and understand the concepts of probability and random variable of the various functions;
- understand the notion of a Markov chain, and how simple ideas of conditional probability and
  matrices can be used to give a thorough and effective account of discrete-time Markov chains;
- To formulate and construct a mathematical model for a linear programming problem in real life
  situation;
- Introduce the Fourier Transform as an extension of Fourier techniques on periodic functions and
to solve partial differential equations;

OUTCOMES:
On successful completion of this course, all students will have developed knowledge and
understanding in the fields of linear algebra, probability, stochastic process, linear programming
problem and fourier transform

UNIT I  LINEAR ALGEBRA (9+3)
Vector spaces – norms – Inner Products – Eigenvalues using QR transformations – QR factorization -
generalized eigenvectors – Canonical forms – singular value decomposition and applications - pseudo
inverse – least square approximations --Toeplitz matrices and some applications.

UNIT II  ONE DIMENSIONAL RANDOM VARIABLES (9+3)
Random variables - Probability function – moments – moment generating functions and their
properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions –
Function of a Random Variable.

UNIT III  RANDOM PROCESSES (9+3)
Classification – Auto correlation - Cross correlation - Stationary random process – Markov process —
Markov chain - Poisson process – Gaussian process.

UNIT IV  LINEAR PROGRAMMING (9+3)
Formulation – Graphical solution – Simplex method – Two phase method - Transportation and
Assignment Models

UNIT V  FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL
EQUATIONS (9+3)
Fourier transforms: Definitions, properties-Transform of elementary functions, Dirac Delta functions –
Convolution theorem – Parseval’s identity – Solutions to partial differential equations: Heat equations,
Wave equations, Laplace and Poison’s equations.

TOTAL: 45+15:60 PERIODS

TEXT BOOKS:
(An imprint of Elsevier), 2010.
New Delhi 2012.
4. Sankara Rao, K. “Introduction to partial differential equations” Prentice Hall of India, pvt, Ltd,
New Delhi, 1997.

REFERENCES:
Hall of India,2006.
cengage learning India private limited.
OBJECTIVES:
The design of all VLSI circuits is carried out by making extensive use Computer Aided Design (CAD) VLSI design tool. Due to continuous scaling of semiconductor technology, most of the VLSI designs employ millions of transistors and circuits of this size can only be carried out with the aid of CAD VLSI design tools. The VLSI design professional needs to have a good understanding of the operation of these CAD VLSI design tools as these are developed primarily for and by the VLSI design professionals. As part of the present introductory course the principles of operation of all the important modules that go into the construction of a complete VLSI CAD tool will be discussed. These include the design flow organization for VLSI, the standard cell based synthesis methodologies for digital VLSI, floor planning and placement principles and related topics will all be covered.

UNIT I VLSI DESIGN METHODOLOGIES

UNIT II DESIGN RULES
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III FLOOR PLANNING
Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION
Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS
High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL : 45 PERIODS

REFERENCES

OUTCOMES:
• In the VLSI industry, the both user and the developer of the VLSI tools must have a firm understanding of how these tools are developed and the constraints and limitation under which they can be operated successfully. After completing this course, students are expected to have completed one of the important prerequisites for professionals in the area of VLSI design.
OBJECTIVE:
This course deals comprehensively with all aspects of transistor level design of all the digital building blocks common to all CMOS microprocessors, DPSs, network processors, digital backend of all wireless systems etc.

The focus will be on the transistor level design and will address all important issues related to size, speed and power consumption. The units are classified according to the important building and will introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.

UNIT I  MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER  12

UNIT II  COMBINATIONAL LOGIC CIRCUITS  9

UNIT III  SEQUENTIAL LOGIC CIRCUITS  9
Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits.

UNIT IV  ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES  9
Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V  INTERCONNECT AND CLOCKING STRATEGIES  9

TOTAL: 45 PERIODS

REFERENCES:

OUTCOMES:
• The student should able to carry out transistor level hand calculation based design of the most important building blocks used in digital CMOS VLSI circuits.
• The student would have developed strong understanding of the design methodology and tradeoffs of the various circuit choices for each of all the blocks discussed.
OBJECTIVES:
The laboratory based study for the entire program is clubbed under three categories. One is the FPGA based design methodology, the second is the simulation of analog building blocks, and analog and digital CAD design flow. Experiments pertaining to the former two topics are covered in this lab course and those pertaining to the latter will be covered in VLSI Design Lab II.

FPGAs are important platforms used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes, the students will be carrying out complete hardware level FPGA validation of important digital algorithms. In addition, exercises on the SPICE simulation of the basic CMOS analog building blocks will be carried out.

OUTCOME:
After completing this course, given a digital system specification, the student should be able to map it onto FPGA platform and carry out a series of validations starting from design entry to hardware testing. In addition, the student also will be able to design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behavior of feedback based circuits and compute the input/output impedances.

Design Entry Using VHDL or Verilog examples for Digital circuit descriptions using HDL languages:
- Understanding Synthesis principles. Back annotation.
- Test vector generation and timing analysis of sequential and combinational logic design realized using HDL languages.
- FPGA real time programming and I/O interfacing.
- Interfacing with Memory modules in FPGA Boards.
- Verification of design functionality implemented in FPGA by capturing the signal in DSO.
- Real time application development.

TOTAL : 60 PERIODS

AP8252 DIGITAL IMAGE PROCESSING L T P C 3 0 2 4

OBJECTIVES
- To understand the techniques for image enhancement.
- To understand techniques for image segmentation.
- To understand the techniques for compression.

OUTCOMES:
- To be able to design and implement image enhancement schemes.
- To be able to design and implement compression schemes.
- To be able to design and implement restoration schemes.
- To be able to design and implement segmentation schemes.

UNIT I IMAGE REPRESENTATION
Image representation-Image Basis Functions- Two dimensional DFT- Discrete Cosine Transform-Walsh- Hadamard transform-Wavelet transform- Principal component analysis.
UNIT II    IMAGE ENHANCEMENT AND RESTORATION  9+6
Gray level transformation techniques- Spatial domain techniques - Half toning, Median filtering, contrast stretching, Histogram Equalization- Frequency domain techniques - Weiner filtering-Homomorphic filtering- PSFs for different forms of blur - noise models- color image processing.

UNIT III  IMAGE SEGMENTATION  9+6
Segmentation - Similarity and dissimilarity methods- Thresholding - Edge based and Region based methods- Hough transform- Morphological operations - Clustering methods.

UNIT IV    IMAGE COMPRESSION  9+6

UNIT V      SIMULATION  9+6

TOTAL: 45+30=75 PERIODS

REFERENCES:

VL8251      DATA CONVERTERS  L T P C  3 0 0 3

OBJECTIVES:
Analog to Digital (AD) and Digital to Analog (DA) converters constitute a very important building block in all electronics systems. It is these blocks which provide the crucial interface between the primarily analog real world signals and the predominantly digital electronic systems.

These are critical blocks which are utilized in all major industrial sectors including computers, wireless communication, audio and video systems, biomedical systems, aerospace and automotive systems and so on. There are a few established circuit architectures and principles for design of AD and DA converters.

The performance limits of both these blocks have been continuously and rapidly improved upon over the last thirty years and this trend is expected to continue at the same pace in the foreseeable future too.

The present course will explain the basic operational and design principles of the most important CMOS AD and DA converter architectures.
**OUTCOMES:**
The student who undergoes this course will be able to carry out the design calculations for developing the various blocks associated with a typical CMOS AD or DA converter, select an appropriate configuration as per the required specifications on overall converter, and eventually arrive at the dimensions and bias conditions of all the MOS transistors involved in the design.

**UNIT I** INTRODUCTION AND CHARACTERISTICS OF AD/DA CONVERTER
CHARACTERISTICS 9
Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and antialiasing filters.

**UNIT II** SWITCH CAPACITOR CIRCUITS AND COMPARATORS 9
Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques

**UNIT III** NYQUIST RATE D/A CONVERTERS 9
Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues in current element matching, clock feed through, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs

**UNIT IV** PIPELINE AND OTHER ADCs 9
Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

**UNIT V** SIGMA DELTA CONVERTERS 9
STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Opamp nonlinearities,

**TOTAL: 45 PERIODS**

**REFERENCES:**
4. R. Schreier, G. Temes, Understanding Delta-Sigma DataConverters, Wiley-IEEE Press, 2004
6. VLSI Data Conversion Circuits EE658 recorded lectures available at http://www.ee.iitm.ac.in/~nagendra/videolecture

**VL8211**

**VLSI DESIGN LABORATORY II**

L T P C 0 0 4 2

**OBJECTIVES:**
The focus of this course the CAD based VLSI design flow. The entire VLSI design industry makes use of this design flow in some for or the other. Proficiency and familiarity with the various stages of this design flow is a prerequisite for any student who wishes to be apart of either the industry or the research in VLSI. Over one full semester, exposure to various stages of a typical ‘state of the art’ CAD VLSI tool be provided by various experiments designed to bring out the key aspects of each important module in the CAD tool including the synthesis, place and route,layout, LVS, simulation, and power and clock routing modules.
OUTCOME:
The student would have hands on experience in carrying out a complete VLSI based experiments using / CADENCE / TANNER / Mentor/Synopsis
ASIC RTL realization of an available open source MCU
To synthesize and understand the Boolean optimization in synthesis.

i. Static Timing analyses procedures and constraints.Critical path considerations.

ii. Scan chain insertion, Floor Planning, Routing and Placement procedures.

iii. Power Planning, Layout generation, LVS and Back annotation, Total power estimate.
    Analog Circuit simulation

iv. Simulation of logic gates, current mirrors, Current Sources, Differential Amplifier in Spice.

v. Layout generation, LVS, Back annotation

TOTAL: 60 PERIODS

VL8001 ADVANCED MOSFET MODELING

OBJECTIVE:
The present and future generation VLSI systems are all expected to be built using MOSFETs. Over the years, the VLSI industry has systematically adapted to the use of only MOSFET for all purposes. This is because of its potential from manufacturability point of view. Over the years, advances in physics has given rise many new concepts including carbon nano tubes, organic electronics, single electron and molecular transistors and so on. Even in most of these and other emerging nanotechnology based systems, the MOSFET or devices with MOSFET like characteristics continue to play a very important role. The present course will introduce and cover in detail all the important techniques used for MOSFET device modeling. This course can be considered as an extension or advanced version of the course on ‘SOLID STATE DEVICE MODELING AND SIMULATION’

OUTCOME:
The student who completes this course will be able to utilize the various MOSFET device models available the various CAD tools, contribute to the development and study of newer models for both existing and emerging newer versions of MOSFET devices.

UNIT I BASIC DEVICE PHYSICS
Intrinsic and extrinsic semiconductors, direct and indirect semiconductors. Electrons and holes in silicon - energy bands, electron and hole densities in equilibrium, Fermi-Dirac statistics, carrier concentration, ionization of impurities. Carrier transport in silicon – drift current, diffusion current. p-n junctions - built-in potential, electric field, current-voltage characteristics.

UNIT II MOSFET DEVICES
MOS capacitors - surface potential, accumulation, depletion, inversion, electrostatic potential and charge distribution, threshold voltage, polysilicon work function, interface states and oxide traps. Long-channel MOSFETs – threshold voltage, substrate bias and temperature dependence of threshold voltage, drain-current model, sub-threshold characteristics, channel mobility, capacitances.

UNIT III NANO-SCALED CLASSICAL MOSFETS
Scaling of MOSFETs – constant-voltage scaling, constant-field scaling. Short-channel MOSFETs – short-channel effects, velocity saturation, channel length modulation, source-drain series resistance, DIBL, GIDL. Variability in MOSFETs. Reliability of MOSFETs - high-field effects, hot carrier degradation, negative-bias temperature instability, MOSFET breakdown, high-k dielectrics.
UNIT IV  NON-CLASSICAL MOSFETs
Need for non-classical MOSFETs, Silicon-On-Insulator MOSFETs- Current-voltage equations, fully-depleted SOI MOSFETs, partially-depleted SOI MOSFETs, Heterostructure MOSFETs - strained-channel MOSFETs, Power MOSFETs - SiC MOSFETs, Silicon Nanowires, Carbon Nanotubes.

UNITY  COMPACT MODELS FOR CIRCUIT SIMULATORS
Introduction to compact models, SPICE Level - 1, 2 and 3 MOS models, BSIM model, EKV model, PSP model, Noise modeling, High-frequency models, Parameter extraction of MOSFETs.

TOTAL: 45 PERIODS

REFERENCES:

VL8002  DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING CIRCUITS

OBJECTIVE:
This course deals with CMOS circuit design of various Analog Filter architectures. The required signal conditioning techniques in a Mixed signal IC environment are also dealt in this course.

OUTCOME:
The student will understand the operational and design principles of all the important active analog filter configurations. The student also will gain working knowledge of signal conditioning techniques and the necessary guidelines in a Mixed signal IC environment.

UNIT I  FILTER TOPOLOGIES
The Bilinear Transfer Function - Active RC Implementation, Transconductor-C Implementation, Switched Capacitor Implementation, Biquadratic Transfer Function, Active RC implementation, Switched capacitor implementation, High Q, Q peaking and instability, Transconductor-C Implementation, The Digital Biquad.

UNIT II  INTEGRATOR REALIZATION

UNIT III  SWITCHED CAPACITOR FILTER REALIZATION
Switched capacitor Technique, Biquadratic SC Filters, SC N-path filters, Finite gain and bandwidth effects, Layout consideration, Noise in SC Filters.

UNIT IV  SIGNAL CONDITIONING TECHNIQUES
Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners for capacitive sensors, Noise and Drift in Resistors, Layout Techniques.
UNIT V SIGNAL CONDITIONING CIRCUITS
Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Transimpedance Amplifiers, Charge Amplifiers, Noise in Amplifiers

TOTAL : 45 PERIODS

REFERENCES:

AP8071 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

OBJECTIVES:
- To expose the students to the fundamentals of microprocessor architecture.
- To introduce the advanced features in microprocessors and microcontrollers.
- To enable the students to understand various microcontroller architectures.

UNIT I MICROPROCESSOR ARCHITECTURE

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM

UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS
Instruction set addressing modes – operating modes – Interrupt system – RTC – Serial Communication Interface – A/D Converter PWM and UART.

UNIT V PIC MICROCONTROLLER

TOTAL : 45 PERIODS

REFERENCES:

Readings: Web links www.ocw.nit.edu  www.arm.com
OUTCOMES:
- The student will be able to work with suitable microprocessor / microcontroller for a specific real world application.

AP8072 ARTIFICIAL INTELLIGENCE AND OPTIMIZATION TECHNIQUES

OBJECTIVES:
- To introduce the techniques of computational methods inspired by nature, such as neural networks, genetic algorithms and other evolutionary computation systems, ant swarm optimization, artificial immune systems, cellular automata, and multi-agent systems.
- To present main rules underlying in these techniques.
- To present selected case-studies.
- To adopt these techniques in solving problems in the real world.

UNIT I NEURAL NETWORKS

UNIT II FUZZY LOGIC SYSTEMS

UNIT III EVOLUTIONARY COMPUTATION AND GENETIC ALGORITHMS

UNIT IV ANT COLONY OPTIMIZATION
Ant Colony Optimization: Introduction – From real to artificial ants- Theoretical considerations – Convergence proofs – ACO Algorithm – ACO and model based search – Application principles of ACO.

UNIT V PARTICLE SWARM OPTIMIZATION

TOTAL: 45 PERIODS

REFERENCES:
1. Christopher M. Bishop, “Neural Networks for Pattern Recognition”, Oxford University Press
7. N P Padhy, Artificial Intelligence and Intelligent Systems, Oxford University Press, 2005

OUTCOMES:
- An understanding of the fundamental Computational Intelligence models
- Understanding the concepts of neural networks, genetic algorithms, fuzzy neural networks, and ant colony optimization algorithms
- Application of computational Intelligence techniques to classification, pattern recognition, prediction, rule extraction, and optimization problems.

AP8073 DESIGN AND ANALYSIS OF ALGORITHMS

OBJECTIVES:
- Discusses the algorithmic complexity parameters and the basic algorithmic design techniques.
- To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms and NP Hard Problems.

UNIT I INTRODUCTION
Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II DESIGN TECHNIQUES
Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III SEARCHING AND SORTING
Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior.

UNIT IV GRAPH ALGORITHMS
Minimum spanning tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm.

UNIT V SELECTED TOPICS

TOTAL: 45 PERIODS

REFERENCES:

OUTCOMES:
- Will be able to apply the suitable algorithm according to the given optimization problem.
- Ability to modify the algorithms to refine the complexity parameters.
OBJECTIVES:
- The students will learn various design steps starting from system specifications to hardware/software implementation and will experience process optimization while considering various design decisions.
- Students will gain design experience with project/case studies using contemporary high-level methods and tools.

UNIT I  SYSTEM SPECIFICATION AND MODELLING  9

UNIT II  HARDWARE/SOFTWARE PARTITIONING  9
The Hardware/Software Partitioning Problem , Hardware-Software Cost Estimation , Generation of the Partitioning Graph , Formulation of the HW/SW Partitioning Problem , Optimization , HW/SW Partitioning based on Heuristic Scheduling , HW/SW Partitioning based on Genetic Algorithms .

UNIT III  HARDWARE/SOFTWARE CO-SYNTHESIS  9
The Co-Synthesis Problem , State-Transition Graph , Refinement and Controller Generation , Distributed System Co-Synthesis

UNIT IV  PROTOTYPING AND EMULATION  9

UNIT V  DESIGN SPECIFICATION AND VERIFICATION  9

TOTAL : 45 PERIODS

REFERENCES:

OUTCOMES:
On completion of the course, a student should be able:
- To understand and to apply design methodologies
- To appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their inter-relationships
- To be familiar with modern hardware/software tools for building prototypes
- To demonstrate practical competence in these areas.
OBJECTIVES:
- To give them hands on experience for the fabrication processes using micro-fabrication tools in the cleanroom.
- Briefly review on various application fields of the microsensors, MEMS, and smart devices. The materials and the processes required to make different kinds of the microdevices.
- The standard microelectronics technology to produce ultra large-scale integrated circuits and package them will also be reviewed. The new techniques that have been developed to make microsensors and microactuators, such as bulk and surface silicon micromachining will be followed.
- The fabrication process will include metal thin film e-beam evaporation, dielectric thin film growing using oxidation tube furnace, electrochemical deposition, and various kinds of chemical processes.

UNIT I   INTRODUCTION TO MEMS
MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II  MECHANICS FOR MEMS DESIGN
Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III ELECTRO STATIC DESIGN
Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV  CIRCUIT AND SYSTEM ISSUES
Electronic Interfaces, Feed back systems, Noise , Circuit and system issues, Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

UNIT V   INTRODUCTION TO OPTICAL AND RF MEMS
Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

TOTAL : 45 PERIODS

TEXT BOOK:

REFERENCES:
OUTCOMES:
On completion of the module students should:
- Be able to extend the principles of microfabrication to the development of micromechanical devices and the design of microsystems
- Understand the principles of energy transduction, sensing and actuation on a microscopic scale.
- Appreciate the effects of scaling, and the similarities and differences between micromechanical assemblies and macroscopic machines.
- Be able to analyse and model the behaviour of microelectromechanical devices and systems

AP8079 NONLINEAR SIGNAL PROCESSING

OBJECTIVES:
- To introduce nonlinear filtering concepts, algorithms and architectures
- To apply these algorithms in image processing

UNIT I INTRODUCTION TO NONLINEAR FILTERS AND STATISTICAL PRELIMINARIES

UNIT II NONLINEAR DIGITAL SIGNAL PROCESSING BASED ON ORDER STATISTICS

UNIT III ADAPTIVE NONLINEAR AND POLYNOMIAL FILTERS

UNIT IV ALGORITHMS AND ARCHITECTURES

UNIT V APPLICATIONS OF NONLINEAR FILTERS
Power spectrum analysis – Morphological image processing – nonlinear edge detection impulse noise rejection in image and bio signals – two component image filtering – speech processing

TOTAL: 45 PERIODS

REFERENCES:
OUTCOMES:
- Know and understand the optimal solution to the filtering problem
- Ability to solve linear and nonlinear filtering problem as applied to signal and image processing

AP8080  RF SYSTEM DESIGN  L T P C  3 0 0 3

OBJECTIVES:
The CMOS RF Front End (RFE) is a very crucial building block and in all of wireless and many high frequency wire-line systems. The RFE has few important building blocks within including the Low Noise Amplifiers, Phase Locked Loop Synthesizers, Mixers, Power Amplifiers, and impedance matching circuits. The present course will introduce the principles of operation and design principles associated with these important blocks. The course will also provide and highlight the appropriate digital communication related design objectives and constraints associated with the RFEs.

OUTCOME:
The student after completing this course must be able to translate the top level wireless communications system specifications into block level specifications of the RFE. The student should also be able to carry out transistor level design of the entire RFE.

UNIT I  CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES
Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter

UNIT II  IMPEDANCE MATCHING AND AMPLIFIERS
S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III  FEEDBACK SYSTEMS AND POWER AMPLIFIERS
Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT IV  MIXERS AND OSCILLATORS
Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V  PLL AND FREQUENCY SYNTHESIZERS
Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers,

TOTAL : 45 PERIODS
TEXT BOOKS:
5. Recorded lectures and notes available at http://www.ee.iitm.ac.in/~ani/ee6240/

AP8081 
SELECTED TOPICS IN ASIC DESIGN 

L T P C 
3 0 0 3 

OBJECTIVE:
The course focuses on the semi custom IC Design and introduces the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles. The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I 
INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 
Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II 
PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III 
PROGRAMMABLE ASIC ARCHITECTURE 

UNIT IV 
LOGIC SYNTHESIS, PLACEMENT AND ROUTING 
Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.

UNIT V 
HIGH PERFORMANCE ALGORITHMS FOR ASICS/ SOCS. SOC CASE STUDIES 

TOTAL : 45 PERIODS

REFERENCES:
OUTCOME:
After completing this course, the student would have gained knowledge in the circuit design aspects at the next transistor and block level abstractions of FPGA and ASIC design. In combination with the course on CAD for VLSI, the student would have gained sufficient theoretical knowledge for carrying out FPGA and ASIC designs.

AP8082 SELECTED TOPICS IN IC DESIGN

OBJECTIVE:
This course deals with the supply circuit modules which are crucial modules in an IC design. Clock generation circuits play a major role in High Speed Broad Band Communication circuits, High Speed I/O’s, Memory modules and Data Conversion Circuits. This course focuses on the design aspect of Clock Generation circuits and their design constraints.

UNIT I VOLTAGE AND CURRENT REFERENCES
Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference, Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II LOW DROP OUT REGULATORS

UNIT III OSCILLATOR FUNDAMENTALS
General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for Ring Oscillators, Phase Noise in Differential LC Oscillators.

UNIT IV PHASE LOCK LOOPS

UNIT V CLOCK AND DATA RECOVERY
CDR Architectures, Tias and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL: 45 PERIODS

REFERENCES:

OUTCOME:
This course provides the essential know how to a designer to construct Supply reference circuits and Clock Generation Circuits for given design specifications and aids the designer to understand the design specifications related to Supply and Clock Generation Circuits.
OBJECTIVES:
- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics.

UNIT I  SIGNAL PROPAGATION ON TRANSMISSION LINES
Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance, wave propagation, reflection, and bounce diagrams. Reactive terminations – L, C, static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline. Reflection and terminations for logic gates, fan-out, logic switching, input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II  MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK
Multi-conductor transmission lines, coupling physics, per unit length parameters. Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip). Differential signalling, termination, balanced circuits, S-parameters, Lossy and Lossless models.

UNIT III  NON-IDEAL EFFECTS

UNIT IV  POWER CONSIDERATIONS AND SYSTEM DESIGN
SSN/SSO, DC power bus design, layer stackup, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed. Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference, Bit-error rate, Timing analysis.

UNIT V  CLOCK DISTRIBUTION AND CLOCK OSCILLATORS
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL : 45 PERIODS

REFERENCES:

TOOLS REQUIRED
1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html

OUTCOMES:
- Ability to identify sources affecting the speed of digital circuits.
- Able to improve the signal transmission characteristics.

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OBJECTIVES:

- To enable the student to understand the role of sensors and the networking of sensed data for different applications.
- To expose the students to the sensor node essentials and the architectural details, the medium access and routing issues and the energy constrained operational scenario.
- To enable the student to understand the challenges in synchronization and localization of sensor nodes, topology management for effective and sustained communication, data management and security aspects.

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS

UNIT II ARCHITECTURES

UNIT III MAC AND ROUTING

UNIT IV INFRASTRUCTURE ESTABLISHMENT
Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT V DATA MANAGEMENT and SECURITY
Data management in WSN, Storage and indexing in sensor networks, Query processing in sensor, Data aggregation, Directed diffusion, Tiny aggregation, greedy aggregation, security in WSN.

TOTAL : 45 PERIODS

REFERENCES:

26
OUTCOMES:
- The student would be able to appreciate the need for designing energy efficient sensor nodes and protocols for prolonging network lifetime.
- The student would be able to demonstrate an understanding of the different implementation challenges and the solution approaches.

OBJECTIVES:
- To introduce methods to analyze and design synchronous and asynchronous sequential circuits
- To introduce variable entered maps and techniques to simplify the Boolean expressions using these maps
- To explain the design procedures for developing complex system controllers using digital ICs

UNIT I 
SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN
Analysis of clocked synchronous sequential circuits – Moore / Mealy State diagrams, State Table, State Reduction and Assignment - Design of synchronous sequential circuits.

UNIT II
ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN
Analysis of asynchronous sequential circuit – Cycles – Races - Static, Dynamic and Essential hazards – Primitive Flow Table - State Reductions and State Assignment - Design of asynchronous sequential circuits.

UNIT III
VEM AND INTRODUCTION TO MULTI-INPUT SYSTEM CONTROLLER DESIGN

UNIT IV
SYSTEM CONTROLLERS USING COMBINATIONAL MSI / LSI CIRCUITS
Decoders and Multiplexers in system controllers – Indirect-Addressed MUX configuration – System controllers using ROM.

UNIT V
SEQUENTIAL AND PROGRAMMABLE SYSTEM CONTROLLERS

TOTAL : 45 PERIODS

REFERENCES:
OUTCOMES:
- Ability to analyze and design sequential digital circuits
- Ability to understand the requirements and specifications of the system required for a given application
- Decide a suitable system controller architecture
- Design system controllers using different digital ICs

AP8153  EMBEDDED SYSTEMS DESIGN  L T P C

OBJECTIVES:
- To expose the students to the fundamentals of embedded system design.
- To enable the students to understand and use embedded computing platform.
- To introduce networking principles in embedded devices.
- To introduce RTOS in embedded devices.

UNIT I  EMBEDDED PROCESSORS

UNIT II  EMBEDDED PROCESSOR AND COMPUTING PLATFORM
Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture

UNIT III  NETWORKS
Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV  REAL-TIME CHARACTERISTICS

UNIT V  SYSTEM DESIGN TECHNIQUES

TOTAL : 45 PERIODS
REFERENCES:

OUTCOME:
Able to select and design suitable embedded systems for real world applications.

AP8251 DIGITAL CONTROL ENGINEERING

OBJECTIVES:
- Students should acquire a fundamental understanding of digital control systems and design.
- To teach the fundamental concepts of Digital Control systems and mathematical modeling of the system.
- To study the concept of time response and frequency response of the discrete time system.
- To teach the basics of stability analysis of the digital system.

UNIT I PRINCIPLES OF CONTROLLERS
Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL
Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM
Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury’s stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS
Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS
Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

TOTAL: 45 PERIODS
REFERENCES:

OUTCOMES:
- Acquire working knowledge of discrete system science-related mathematics.
- Design a discrete system, component or process to meet desired needs.
- Identify, formulate and solve discrete control engineering problems.
- Use the techniques, tools and skills related to discrete signals, computer science and modern discrete control engineering in modern engineering practice
- Communicate system related concepts effectively

IF8151 ADVANCED COMPUTER ARCHITECTURE L T P C
3 0 0 3

OBJECTIVES:
- To understand the evolution of computer architecture.
- To understand the state-of-the-art in computer architecture.
- To understand the design challenges in building a system.

UNIT I PIPELINING AND ILP

UNIT II THREAD-LEVEL PARALLELISM
Multi-threading - Multiprocessors - Centralized and Distributed Shared Memory Architectures - Cache Coherence Issues - Performance Issues - Synchronization Issues - Models of Memory Consistency - Interconnection Networks - Buses, Crossbar and Multi-Stage Switches - Multi-Core Processor Architectures - Case Study.

UNIT III SIMD AND GPU ARCHITECTURES
SIMD Extensions for Multimedia - Graphics Processing Units - GPU Computational Structures - GPY ISA - GPU Memory Structures - Case Study.

UNIT IV MEMORY HIERARCHY DESIGN
Introduction - Optimizations of Cache Performance - Memory Technology and Optimizations - Name Mapping Implementations - Virtual Memory and Virtual Machines - Design of Memory Hierarchies - Case Studies.

UNIT V WAREHOUSE-SCALE COMPUTERS
Programming Models and Workloads - Storage Architectures - Physical Infrastructure - Cloud Infrastructure - Case Study

TOTAL: 45 PERIODS
OUTCOMES:
At the end of the course, the student will be able to:
- Compare and evaluate the performance of various architectures.
- Design sub-systems to meet specific performance requirements.
- Analyze the requirements of large systems to select and build the right infrastructure.

REFERENCES:

VL8071 LOW POWER VLSI DESIGN

OBJECTIVES:
- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

UNIT I POWER DISSIPATION IN CMOS
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION
Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS
Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION
Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER
Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

REFERENCES:

OUTCOMES:
- The student will get to know the basics and advanced techniques in low power design which is a hot topic in today’s market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

VL8072 SOLID STATE DEVICE MODELING AND SIMULATION  L  T  P  C  3 0 0 3

OBJECTIVES:
The three areas of circuit design, device modeling and CAD tools are the main pillars based on which all VLSI system designs are carried out. This course introduces the principles of device modeling wherein device physics and experimentally observed device performance characteristics combined so as to lead to predictable equations and expressions for device performance under various scenarios of excitation. The most widely used device models used by the industry including BSIM and EKV models discussed.

OUTCOME:
The student who completes this course will be in a position understand the procedures used to construct the complicated device models that are widely used in VLSI CAD tools. As the CMOS technology progresses, the student will be in a position to understand the changes introduced in the device models as well as contribute to the development of appropriate device models.

UNIT I MOSFET DEVICE PHYSICS 9
Band theory of solids, carrier transport mechanism, MOS capacitor - surface potential accumulation, depletion, inversion, electrostatic potential and charge distribution, threshold voltage, polysilicon work function, interface states and oxide traps, drain current model, sub-threshold characteristics.

UNIT II MOSFET MODELING 9
Basic modeling, SPICE Level-1, 2 and 3 models, Short channel effects, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling.

UNIT III NOISE MODELING 9
Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuit.

UNIT IV BSIM4 MOSFET MODELING 9
Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, Mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, Noise model, Junction diode models, Layout-dependent parasitics model.
UNIT V  OTHER MOSFET MODELS

The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, Noise model, temperature effects, MOS model 9, MOSAI model, PSP model, Influence of process variation, Modeling of device mismatch for Analog/RF Applications.

TOTAL: 45 PERIODS

REFERENCES

VL8073  TESTING OF VLSI CIRCUITS  L  T  P  C
3  0  0  3

OBJECTIVE:
In the VLSI design industry, a significant portion of work force and resources are been deployed in the test and validation of VLSI designs. The complexity of multimillion transistor based VLSI design calls for special techniques for efficiently testing and validating the VLSI design across all possible input, supply, speed and process corners. This has given rise to systematic areas of study in the form of design for test, automatic test pattern generation, fault diagnosis and these have all become very important areas from both research as well as routine industrial practice point of view.

The present course will introduce the student to the mathematical and scientific principles based on which systematic test and validation can be carried out on multimillion transistor VLSI design.

OUTCOME:
The student who completes this course will be familiar with the principles used in the construction VLSI Design For Test (DFT) tools.

The student will be able to adapt these to his specific industrial needs, also contribute to the development of more efficient tools from the fault coverage and speed point of view.

UNIT I  BASICS OF TESTING AND FAULT MODELLING

UNIT II  TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS
Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.

UNIT III  DESIGN FOR TESTABILITY
Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches.

UNIT IV  SELF-TEST AND TEST ALGORITHMS
built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.
UNIT V  FAULT DIAGNOSIS
Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits -
Self-checking design - System Level Diagnosis.

TOTAL: 45 PERIODS

REFERENCES:
1. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico
3. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-
4. A.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice all

VL8074  VLSI SIGNAL PROCESSING

OBJECTIVES:
- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I  INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL
   PROCESSING OF FIR FILTERS
Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical
path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of
FIR filters, Pipelining and Parallel processing for low power.

UNIT II  RETIMING, ALGORITHMIC STRENGTH REDUCTION
Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding,
sample period reduction and parallel processing application, Algorithmic strength reduction in filters
and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters,
Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III  FAST CONVOLUTION, PIPELINING AND PARALLEL
   PROCESSING OF IIR FILTERS
Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel
recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2
decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining
and parallel processing of IIR filters.

UNIT IV  BIT-LEVEL ARITHMETIC ARCHITECTURES
Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and
carry-save multipliers, Design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter,
CSD representation, CSD multiplication using Horner’s rule for precision improvement, Distributed
Arithmetic fundamentals and FIR filters

UNIT V  NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE
   AND ASYNCHRONOUS PIPELINING
Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative
matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase
clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail
protocol.

TOTAL: 45 PERIODS
REFERENCES:

OUTCOME:
1. Ability to modify the existing or new DSP architectures suitable for VLSI.