VISION OF DEPARTMENT OF ELECTRONICS ENGINEERING

The Department of Electronics Engineering is committed to produce globally competitive and socially sensitized graduates in Electronics & Communication Engineering. We seek to instill the spirit of creativity and leadership skills enabling the students to make a global impact towards the availability of technology to mankind from all walks of life.

MISSION OF DEPARTMENT OF ELECTRONICS ENGINEERING

- To impart high quality technical education to students from socially and economically diverse backgrounds
- Give solid foundation on Mathematical skills and allied fields of Electronics & Communication
- To produce students with technical competence to design sophisticated systems in Electronics & Communication
- To make high quality research contribution in the field of Electronics, Communication, Networking, VLSI & Signal Processing
- To collaborate with industries in Electronics & Communication in the indigenous product development
- To inculcate qualities of leadership and entrepreneurship in students
- To facilitate adequate exposure to the faculty enabling them to be synchronized with the Cutting edge technology
1. PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):
   
   I. Enrich students to excel in research leading to cutting edge technology in VLSI design and Embedded Systems and creating competent, innovative, and productive professionals in this field.
   
   II. Provide students with a solid foundation in MOS devices, digital electronics design, analog system design and computer architecture principles leading to VLSI design.
   
   III. Understand the various applications and employ Embedded Systems based solutions to them with good scientific and engineering knowledge so as to comprehend, analyze, design, and create novel products for real life problems.
   
   IV. Provide dynamic diverse academic environment to the students and aware of excellence, leadership, ethical conduct, positive attitude, societal responsibilities and lifelong learning needed for a successful professional career.
   
   V. Inculcate entrepreneurial skills to start industries related to VLSI design and embedded system technologies.

2. PROGRAMME OUTCOMES (POs):

<table>
<thead>
<tr>
<th>PO#</th>
<th>Graduate Attribute</th>
<th>Programme Outcome</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Research aptitude</td>
<td>An ability to independently carry out research /investigation and development work to solve practical problems.</td>
</tr>
<tr>
<td>2.</td>
<td>Technical documentation</td>
<td>An ability to write and present a substantial technical report/document</td>
</tr>
<tr>
<td>3.</td>
<td>Technical competence</td>
<td>Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program</td>
</tr>
<tr>
<td>4.</td>
<td>Engineering Design</td>
<td>Ability to design and conduct experiments, perform analysis, applying the knowledge of computing, mathematics, science and electronic engineering for designing VLSI and Embedded Systems.</td>
</tr>
<tr>
<td>5.</td>
<td>Conduct investigations of complex problems</td>
<td>Interpret the problems of VLSI and Embedded Systems and investigate solutions and work towards improved solutions.</td>
</tr>
<tr>
<td>6.</td>
<td>Life-long Learning</td>
<td>Continuously update knowledge with modern tools and technical developments and ensure professional development.</td>
</tr>
</tbody>
</table>
3. PROGRAMME SPECIFIC OUTCOMES (PSOs):

By the completion of VLSI Design and Embedded Systems programme, students will have the following programme specific outcomes

I. Foundation of VLSI systems: Ability to understand the fundamentals of VLSI systems. Students can assess the basic components and modules of VLSI systems.

II. Foundation of Embedded Systems: Ability to understand the basic principles of Embedded Systems. Students can assess the basic components and modules of Embedded Systems.

III. Foundation of Mathematical concepts: Ability to apply mathematical knowledge to solve complex computations related to the field of VLSI and Embedded Systems.

IV. Applications of VLSI Design and Research ability: Ability to use knowledge in various domains to identify research gaps and hence provide solutions with innovation.

V. Identify the research gaps and provide innovative solutions.

4. PEO/PO Mapping:

<table>
<thead>
<tr>
<th>PEO</th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>I.</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>II.</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>III.</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>7.</td>
</tr>
<tr>
<td>IV.</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>V.</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

L – Low, M – Medium, H - High
| Year | Sem | Courses | | | | | Program Outcomes |
|------|-----|---------|---|---|---|---|---|---|---|---|---|
|      |     |         | PO01 | PO02 | PO03 | PO04 | PO05 | PO06 |
| First| I   | Advanced Applied Mathematics | L   | H    | H    | L    | L    |     |
|      |     | Digital Integrated Circuit Design | H   | M    | H    | H    | H    | H    |
|      |     | VLSI Architectures for System Design | H   | M    | H    | H    | H    | H    |
|      |     | Advanced Embedded System Design | H   | M    | H    | H    | H    | H    |
|      |     | Real Time Embedded System Design | L   | M    | H    | H    | L    | H    |
|      |     | Research Methodology and IPR | H   | H    |     |     |     |     |
|      |     | Audit Course- I |     |     |     |     |     |     |
|      |     | Digital System Design Lab | H   | H    | H    | H    | H    | H    |
|      |     | Embedded Systems Lab | H   | H    | H    | H    | H    | H    |
|      | II  | Design for Testability | H   | H    | H    | H    | H    | H    |
|      |     | CMOS analog IC Design | H   | M    | H    | H    | H    | H    |
|      |     | Hardware-Software Co-design of Embedded system | H   | M    | H    | H    | H    | H    |
|      |     | Embedded Automation | H   | M    | H    | H    | H    | H    |
|      |     | Program Elective Course - I |     |     |     |     |     |     |
|      |     | Audit Course - II |     |     |     |     |     |     |
|      |     | Analog System Design Lab | H   | H    | H    | H    | H    | H    |
|      |     | Embedded Automation Lab | H   | H    | H    | H    | H    | H    |
|      |     | Mini Project with Seminar | H   | H    | H    | H    | H    | H    |
| Second| III | Program Elective Course – II |     |     |     |     |     |     |
|      |     | Program Elective Course – III |     |     |     |     |     |     |
|      |     | Program Elective Course – IV |     |     |     |     |     |     |
|      |     | Open Elective |     |     |     |     |     |     |
|      |     | Dissertation - I | H   | H    | H    | H    | H    | H    |
|      | IV  | Dissertation - II | H   | H    | H    | H    | H    | H    |

Page 4 of 84
<table>
<thead>
<tr>
<th>S. No.</th>
<th>Program Elective Courses</th>
<th>Program Outcomes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.</td>
<td>VLSI Signal Processing Techniques</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>3.</td>
<td>VLSI For Wireless Communication</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>4.</td>
<td>Low Power VLSI Design</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>5.</td>
<td>ASIC Design</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>7.</td>
<td>Network on Chip Design</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>8.</td>
<td>Advanced CMOS Analog IC Design</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>9.</td>
<td>Reconfigurable Architectures and Applications</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>11.</td>
<td>Digital Signal Processors and Architectures</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>12.</td>
<td>Multi-Core Architectures and Programming</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>13.</td>
<td>Image Analysis and Computer Vision</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>14.</td>
<td>Quantum Computing</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>17.</td>
<td>Distributed Embedded Computing</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>18.</td>
<td>Embedded Networking</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>20.</td>
<td>Embedded C Programming</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>22.</td>
<td>MEMS and Microsystems</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>23.</td>
<td>RF IC Design</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>24.</td>
<td>Computational Intelligence</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
<tr>
<td>25.</td>
<td>Robotics</td>
<td>PO01: H, PO02: M, PO03: H, PO04: H, PO05: H, PO06: H</td>
</tr>
</tbody>
</table>
## ANNA UNIVERSITY: CHENNAI
### UNIVERSITY DEPARTMENTS
#### M.E. VLSI DESIGN AND EMBEDDED SYSTEMS
##### REGULATIONS 2019
###### I – IV SEMESTER CURRICULA AND SYLLABI

### SEMESTER – I

<table>
<thead>
<tr>
<th>S. NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td><strong>THEORY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td>MA5159</td>
<td>Advanced Applied Mathematics</td>
<td>FC</td>
<td>3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2.</td>
<td>VE5101</td>
<td>Digital Integrated Circuit Design</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3.</td>
<td>VE5102</td>
<td>VLSI Architectures for System Design</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4.</td>
<td>VE5103</td>
<td>Advanced Embedded System Design</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5.</td>
<td>VE5104</td>
<td>Real Time Embedded System Design</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6.</td>
<td>RM5151</td>
<td>Research Methodology and IPR</td>
<td>RMC</td>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7.</td>
<td></td>
<td>Audit Course- I*</td>
<td>AC</td>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td><strong>PRACTICALS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.</td>
<td>VE5111</td>
<td>Digital System Design Lab</td>
<td>PCC</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>9.</td>
<td>VE5112</td>
<td>Embedded Systems Lab</td>
<td>PCC</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
</tbody>
</table>

**TOTAL** | 19 | 1 | 8 | 28 | 22 |

*Audit Course is Optional*
# SEMESTER – II

<table>
<thead>
<tr>
<th>S.NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td>THEORY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td>VE5201</td>
<td>Design for Testability</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2.</td>
<td>VE5251</td>
<td>CMOS Analog IC Design</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3.</td>
<td>VE5202</td>
<td>Hardware-Software Co-design of Embedded system</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4.</td>
<td>VE5203</td>
<td>Embedded Automation</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5.</td>
<td></td>
<td>Program Elective I</td>
<td>PEC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6.</td>
<td></td>
<td>Audit Course – II*</td>
<td>AC</td>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>PRACTICALS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7.</td>
<td>VE5211</td>
<td>Analog System Design Lab</td>
<td>PCC</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>8.</td>
<td>VE5212</td>
<td>Embedded Automation Lab</td>
<td>PCC</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>9.</td>
<td>VE5213</td>
<td>Mini Project with Seminar</td>
<td>EEC</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td>17</td>
<td>0</td>
<td>12</td>
</tr>
</tbody>
</table>

*Audit Course is Optional

# SEMESTER – III

<table>
<thead>
<tr>
<th>S.NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td>THEORY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td></td>
<td>Program Elective II</td>
<td>PEC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2.</td>
<td></td>
<td>Program Elective III</td>
<td>PEC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3.</td>
<td></td>
<td>Program Elective IV</td>
<td>PEC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4.</td>
<td></td>
<td>Open Elective</td>
<td>OEC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>PRACTICALS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.</td>
<td>VE5311</td>
<td>Dissertation- I</td>
<td>EEC</td>
<td>0</td>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td>12</td>
<td>0</td>
<td>12</td>
</tr>
</tbody>
</table>

Page 7 of 84
## SEMESTER – IV

<table>
<thead>
<tr>
<th>S. NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td>0</td>
<td>0</td>
<td>24</td>
</tr>
</tbody>
</table>

TOTAL NO. OF CREDITS: 73

### ANNA UNIVERSITY, CHENNAI
UNIVERSITY DEPARTMENTS
M.E. VLSI DESIGN AND EMBEDDED SYSTEMS
REGULATIONS 2019
I TO VI SEMESTERS CURRICULA AND SYLLABI (PART – TIME)

## SEMESTER – I

<table>
<thead>
<tr>
<th>S. NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>THEORY</strong></td>
<td></td>
<td>3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>PRACTICALS</strong></td>
<td></td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td>11</td>
<td>1</td>
<td>4</td>
</tr>
</tbody>
</table>

*Audit Course is Optional*
### SEMESTER – II

<table>
<thead>
<tr>
<th>S. NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td><strong>THEORY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td>VE5201</td>
<td>Design for Testability</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2.</td>
<td>VE5251</td>
<td>CMOS Analog IC Design</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3.</td>
<td>VE5202</td>
<td>Hardware-Software Co-design of Embedded system</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4.</td>
<td></td>
<td>Audit Course – II*</td>
<td>AC</td>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td><strong>PRACTICALS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.</td>
<td>VE5211</td>
<td>Analog System Design Lab</td>
<td>PCC</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td></td>
<td>11</td>
<td>0</td>
<td>4</td>
</tr>
</tbody>
</table>

*Audit course is optional

### SEMESTER – III

<table>
<thead>
<tr>
<th>S. NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td><strong>THEORY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td>VE5102</td>
<td>VLSI Architectures for System Design</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2.</td>
<td>VE5104</td>
<td>Real Time Embedded System Design</td>
<td>PCC</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3.</td>
<td>RM5151</td>
<td>Research Methodology and IPR</td>
<td>RMC</td>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td><strong>PRACTICALS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>VE5112</td>
<td>Embedded Systems Lab</td>
<td>PCC</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>0</td>
<td>4</td>
</tr>
</tbody>
</table>
### SEMESTER – IV

<table>
<thead>
<tr>
<th>S. No.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Theory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td>VE5203</td>
<td>Embedded Automation</td>
<td>PCC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>2.</td>
<td></td>
<td>Program Elective I</td>
<td>PEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>3.</td>
<td></td>
<td>Program Elective II</td>
<td>PEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PRACTICALS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>VE5212</td>
<td>Embedded Automation Lab</td>
<td>PCC</td>
<td>0 0 4</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>5.</td>
<td>VE5213</td>
<td>Mini Project with Seminar</td>
<td>EEC</td>
<td>0 0 4</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TOTAL</td>
<td></td>
<td>9 0 8</td>
<td>17</td>
<td>13</td>
</tr>
</tbody>
</table>

### SEMESTER – V

<table>
<thead>
<tr>
<th>S. No.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Theory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td></td>
<td>Program Elective III</td>
<td>PEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>2.</td>
<td></td>
<td>Program Elective IV</td>
<td>PEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>3.</td>
<td></td>
<td>Open Elective</td>
<td>OEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PRACTICALS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>VE5311</td>
<td>Dissertation - I</td>
<td>EEC</td>
<td>0 0 12</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TOTAL</td>
<td></td>
<td>9 0 12</td>
<td>21</td>
<td>15</td>
</tr>
</tbody>
</table>

### SEMESTER – VI

<table>
<thead>
<tr>
<th>S. No.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>PRACTICALS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td>VE5411</td>
<td>Dissertation - II</td>
<td>EEC</td>
<td>0 0 24</td>
<td>24</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TOTAL</td>
<td></td>
<td>0 0 24</td>
<td>24</td>
<td>12</td>
</tr>
</tbody>
</table>

TOTAL NO. OF CREDITS: 73
### PROFESSIONAL CORE COURSES (PCC)

<table>
<thead>
<tr>
<th>S. NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VE5101</td>
<td>Digital Integrated Circuit Design</td>
<td>PCC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>VE5102</td>
<td>VLSI architectures for system design</td>
<td>PCC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>VE5103</td>
<td>Advanced Embedded System Design</td>
<td>PCC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>VE5104</td>
<td>Real Time Embedded System Design</td>
<td>PCC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>VE5201</td>
<td>Design for Testability</td>
<td>PCC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>VE5251</td>
<td>CMOS Analog IC Design</td>
<td>PCC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>VE5202</td>
<td>Hardware-Software Co-design of Embedded system</td>
<td>PCC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>VE5203</td>
<td>Embedded Automation</td>
<td>PCC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>9</td>
<td>VE5111</td>
<td>Digital System Design Lab</td>
<td>PCC</td>
<td>0 0 4</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>10</td>
<td>VE5112</td>
<td>Embedded Systems Lab</td>
<td>PCC</td>
<td>0 0 4</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>11</td>
<td>VE5211</td>
<td>Analog System Design Lab</td>
<td>PCC</td>
<td>0 0 4</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>12</td>
<td>VE5212</td>
<td>Embedded Automation Lab</td>
<td>PCC</td>
<td>0 0 4</td>
<td>4</td>
<td>2</td>
</tr>
</tbody>
</table>

### FOUNDATION COURSES (FC)

<table>
<thead>
<tr>
<th>S.NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT PERIODS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MA5159</td>
<td>Advanced Applied Mathematics</td>
<td>FC</td>
<td>3 1 0</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>
### EMPLOYABILITY ENHANCEMENT COURSES (EEC)

<table>
<thead>
<tr>
<th>S.NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT Periods</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>VE5311</td>
<td>Dissertation - I</td>
<td>EEC</td>
<td>0 0 12</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td>2.</td>
<td>VE5411</td>
<td>Dissertation - II</td>
<td>EEC</td>
<td>0 0 24</td>
<td>24</td>
<td>12</td>
</tr>
<tr>
<td>3.</td>
<td>VE5213</td>
<td>Mini Project with Seminar</td>
<td>EEC</td>
<td>0 0 4</td>
<td>4</td>
<td>2</td>
</tr>
</tbody>
</table>

### RESEARCH METHODOLOGY AND IPR COURSES (RMC)

<table>
<thead>
<tr>
<th>S. NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT Periods</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>RM5151</td>
<td>Research Methodology and IPR</td>
<td>RMC</td>
<td>2 0 0</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

### OPEN ELECTIVE COURSES (OEC)

<table>
<thead>
<tr>
<th>S.NO.</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>CATEGORY</th>
<th>PERIODS PER WEEK</th>
<th>TOTAL CONTACT Periods</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>OE5091</td>
<td>Business Data Analytics</td>
<td>OEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>2.</td>
<td>OE5092</td>
<td>Industrial Safety</td>
<td>OEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>3.</td>
<td>OE5093</td>
<td>Operations Research</td>
<td>OEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>4.</td>
<td>OE5094</td>
<td>Cost Management of Engineering Projects</td>
<td>OEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>5.</td>
<td>OE5095</td>
<td>Composite Materials</td>
<td>OEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>6.</td>
<td>OE5096</td>
<td>Waste to Energy</td>
<td>OEC</td>
<td>3 0 0</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>
AUDIT COURSES (AC)
Registration for any of these courses is optional to students

<table>
<thead>
<tr>
<th>SL. NO</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>PERIODS PER WEEK</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Lecture</td>
<td>Tutorial</td>
</tr>
<tr>
<td>1.</td>
<td>AX5091</td>
<td>English for Research Paper Writing</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>2.</td>
<td>AX5092</td>
<td>Disaster Management</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3.</td>
<td>AX5093</td>
<td>Sanskrit for Technical Knowledge</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>4.</td>
<td>AX5094</td>
<td>Value Education</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>5.</td>
<td>AX5095</td>
<td>Constitution of India</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>6.</td>
<td>AX5096</td>
<td>Pedagogy Studies</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>7.</td>
<td>AX5097</td>
<td>Stress Management by Yoga</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>8.</td>
<td>AX5098</td>
<td>Personality Development Through Life Enlightenment Skills</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>9.</td>
<td>AX5099</td>
<td>Unnat Bharat Abhiyan</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total Credits</strong></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>S.NO.</td>
<td>COURSE CODE</td>
<td>COURSE TITLE</td>
<td>CATEGORY</td>
<td>PERIODS PER WEEK</td>
</tr>
<tr>
<td>-------</td>
<td>-------------</td>
<td>--------------------------------------------------</td>
<td>----------</td>
<td>------------------</td>
</tr>
<tr>
<td>1.</td>
<td>VE5001</td>
<td>Solid State Device Modeling</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>2.</td>
<td>VE5071</td>
<td>VLSI Signal Processing Techniques</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>3.</td>
<td>VE5002</td>
<td>VLSI For Wireless Communication</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>4.</td>
<td>VL5251</td>
<td>Low Power VLSI Design</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>5.</td>
<td>VL5151</td>
<td>ASIC Design</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>6.</td>
<td>VE5003</td>
<td>SoC Design for Embedded System</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>7.</td>
<td>VE5004</td>
<td>Network on Chip Design</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>8.</td>
<td>VE5005</td>
<td>Advanced CMOS Analog IC Design</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>9.</td>
<td>NE5079</td>
<td>Reconfigurable Architectures and Applications</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>10.</td>
<td>VE5006</td>
<td>Computer Aided Design for VLSI Systems</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>11.</td>
<td>VE5007</td>
<td>Digital Signal Processors and Architectures</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>12.</td>
<td>VE5008</td>
<td>Multi-Core Architectures and Programming</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>13.</td>
<td>NE5074</td>
<td>Image Analysis and Computer Vision</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>14.</td>
<td>VE5009</td>
<td>Quantum Computing</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>15.</td>
<td>NE5251</td>
<td>Adaptive Signal Processing Techniques</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>16.</td>
<td>NE5078</td>
<td>Pattern Recognition and Machine Learning</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>17.</td>
<td>VE5010</td>
<td>Distributed Embedded Computing</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td>18.</td>
<td>VE5011</td>
<td>Embedded Networking</td>
<td>PEC</td>
<td>3 0 0</td>
</tr>
<tr>
<td></td>
<td>Course Code</td>
<td>Course Title</td>
<td>Degree</td>
<td>Credits</td>
</tr>
<tr>
<td>---</td>
<td>-------------</td>
<td>----------------------------------------</td>
<td>--------</td>
<td>---------</td>
</tr>
<tr>
<td>19.</td>
<td>VE5012</td>
<td>Real Time Operating Systems</td>
<td>PEC</td>
<td>3</td>
</tr>
<tr>
<td>20.</td>
<td>VE5013</td>
<td>Embedded C Programming</td>
<td>PEC</td>
<td>3</td>
</tr>
<tr>
<td>21.</td>
<td>VE5014</td>
<td>Embedded Automotive Systems</td>
<td>PEC</td>
<td>3</td>
</tr>
<tr>
<td>22.</td>
<td>VE5015</td>
<td>MEMS and Microsystems</td>
<td>PEC</td>
<td>3</td>
</tr>
<tr>
<td>23.</td>
<td>VE5016</td>
<td>RF IC Design</td>
<td>PEC</td>
<td>3</td>
</tr>
<tr>
<td>24.</td>
<td>NE5071</td>
<td>Computational Intelligence</td>
<td>PEC</td>
<td>3</td>
</tr>
<tr>
<td>25.</td>
<td>VE5017</td>
<td>Robotics</td>
<td>PEC</td>
<td>3</td>
</tr>
</tbody>
</table>
MA5159  ADVANCED APPLIED MATHEMATICS   L T P C
3 1 0 4

OBJECTIVES:

- To encourage students to develop a working knowledge of the central ideas of linear algebra.
- To enable students to understand the concepts of probability and random variables.
- To make students understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete-time Markov chains.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in real life situation.
- To introduce the Fourier Transform as an extension of Fourier techniques on periodic functions and to solve partial differential equations.

UNIT I  LINEAR ALGEBRA


UNIT II  ONE DIMENSIONAL RANDOM VARIABLES


UNIT III  RANDOM PROCESSES

Classification – Auto correlation - Cross correlation - Stationary random process – Markov process — Markov chain - Poisson process – Gaussian process.

UNIT IV  LINEAR PROGRAMMING

Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

UNIT V  FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS


TOTAL: 45+15=60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

- Apply the concepts of linear algebra to solve practical problems.
- Use the ideas of probability and random variables in solving engineering problems.
- Classify various random processes and solve problems involving stochastic processes.
- Formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
- Apply the Fourier transform methods of solving standard partial differential equations.
REFERENCES:
   Prentice Hall of India, New Delhi, 2006.
   Boston, 2014.

VE5101  DIGITAL INTEGRATED CIRCUIT DESIGN  L T P C
                                          3 0 0 3

OBJECTIVES:
- To learn the fundamentals of VLSI design
- To understand the transistor level design of combinational and sequential logic circuits
- To study various memory architectures
- To learn the various arithmetic circuits for data path subsystems
- To familiarize the implementation strategies of FPGA architectures

UNIT - I  MOS TRANSISTOR PRINCIPLES  9
MOS Technology and VLSI, CMOS fabrication process and Electrical properties of CMOS circuits –
Secondary effects – Device modeling – Process variations – Static and Dynamic behavior of CMOS

UNIT - II  COMBINATIONAL LOGIC CIRCUITS  9
Static CMOS logic design - Complementary CMOS – Ratioed logic – Pass transistor Logic. Dynamic
CMOS logic – principles – speed and power dissipation – signal integrity issues – cascading dynamic
gates.

UNIT – III  SEQUENTIAL LOGIC CIRCUITS AND MEMORY ARRAY  9
STRUCTURES
Static and Dynamic Latches and Registers, Timing Issues, Pipelines, Clocking strategies, Memory
Architectures, and Memory control circuits.

UNIT – IV  DATAPATH SUBSYSTEMS  9
Introduction – Addition/Subtraction – One/Zero detectors – Comparators – Counters – Coding –
Shifters – Multiplication – Division – Parallel-Prefix Computations.

UNIT – V  IMPLEMENTATION STRATEGIES  9
DIGITAL: Full custom and semicustom design – cell based design – array based implementation -
Programmable ASIC logic cells - ACTEL ACT - Xilinx LCA - Altera FLEX and MAX.

TOTAL: 45 PERIODS
COURSE OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the basics of VLSI design
CO2: Design CMOS combinational and sequential circuits
CO3: Design and analyze various memory architectures
CO4: Analyze characteristics of the datapath/arithmetic circuits
CO5: Analyze Logic block and routing architectures of various FPGAs.

REFERENCES:

<table>
<thead>
<tr>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

VE5102 VLSI ARCHITECTURES FOR SYSTEM DESIGN

OBJECTIVES:
- To introduce the features of programmable logic devices
- To learn the features of various FPGAs and FPAA
- To understand the concepts of synchronous and asynchronous FSMs
- To provide the system design experience with FSMs using PLDs
- To introduce pulse mode approach to asynchronous FSM

UNIT - I PROGRAMMABLE LOGIC DEVICES
Logic implementation options - Technology trends - Design with Field Programmable devices - ROM, PLA, PAL - CPLD - XC9500 family - Erasable Programmable Logic Devices - MAX5000, MAX7000 families.
UNIT - II FPGA AND FPAA

UNIT – III SYNCHRONOUS FSM DESIGN
Choice of Components to be Considered - Architecture Centered around Nonregistered PLDs - State Machine Designs - Centered around a Shift Register, Centered around a Parallel Loadable Up/Down Counter - One hot design method - Use of Algorithmic State Machine, Application of one hot design to serial 2’s complementer, parallel to serial adder/subtractor controller- System-level design: controller, data path, and functional partition.

UNIT – IV ASYNCHRONOUS STATE MACHINE DESIGN
Features and need for Asynchronous FSMs - Lumped path delay models for asynchronous FSMs - Excitation table, state diagrams, K-maps, and state tables - Design of the basic cells by using the LPD model - design examples - Hazards in Asynchronous FSMs - One-hot design of asynchronous state machines - Design of fundamental mode FSMs by using PLDs.

UNIT – V PULSE MODE APPROACH TO ASYNCHRONOUS FSM DESIGN
Pulse Mode Models and System Requirements - Choice of Memory Elements - Other Characteristics of Pulse Mode FSMs - Design Examples - Analysis of Pulse Mode FSMs - One-Hot Programmable Asynchronous Sequencers.

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Implement the digital designs with programmable logic devices
CO2: Analyze the architectural features of FPGA and FPAA
CO3: Make the system level designs using synchronous and asynchronous FSMs
CO4: Design the fundamental mode FSMs using PLDs
CO5: Apply pulse mode approach to FSM Design

REFERENCES:
OBJECTIVES:

- To learn the PIC microcontroller and ARM processor architecture, features, pin details and ASM programming
- To develop the programming skills on PIC microcontroller and ARM Processor
- To understand the concepts of real time operating systems
- To learn the interfacing mechanism of peripheral devices with controllers
- To learn the design and development of real-time embedded system

UNIT - I
INTRODUCTION


UNIT - II
8-BIT CONTROLLER


UNIT – III
32-BIT CONTROLLER


UNIT – IV
INTERFACING PERIPHERAL DEVICES

Embedded C Programming - LED - LCD - Seven Segment Display - Motor (DC, Stepper, Servo) - Relay - Keypad - Keyboard - Sensors - Serial Communication Protocols (I2C, SPI, USART, CAN), Parallel Communication Protocols (PCI, ISA), Global Positioning System

UNIT – V
REAL-TIME OPERATING SYSTEM


TOTAL: 45 PERIODS
OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the PIC microcontroller and ARM Processor architectures
CO2: Write the ASM programming for PIC microcontroller and ARM Processor
CO3: Design the scheduling strategies and resource allocation in RTOS
CO4: Design and develop the hardware and software portion in Real-time embedded Systems
CO5: Port an operating system in Embedded Systems

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VE5104 REAL TIME EMBEDDED SYSTEM DESIGN

OBJECTIVES:
- To understand the basics of embedded system and ARM architecture
- To understand the RTOS concepts like scheduling and memory management related to the embedded system
- To learn about the programming aspects of RTOS
- To learn the different protocols of embedded wireless application
- To understand concepts involved in the design of hardware and software components for an embedded system
UNIT I  INTRODUCTION  9
Computing – Information Access Devices – Smart Cards – Microcontrollers – ARM Processor -Real
time Microcontrollers.

UNIT II  EMBEDDED/REAL TIME OPERATING SYSTEM  9
Operating System Concepts: Processes, Threads, Interrupts, Events - Real Time Scheduling
Algorithms - Memory Management – Overview of Operating Systems for Embedded, Real Time
Handheld Devices – Target Image Creation – Programming in Linux, RTLinux, VxWorks,
Microcontroller operating system overview.

UNIT III  CONNECTIVITY  9
Wireless Connectivity - Bluetooth – Other short Range Protocols – Wireless Application Environment
– Service Discovery – Middleware.

UNIT IV  REAL TIME UML  9
Requirements Analysis – Object Identification Strategies – Object Behaviour – Real Time Design
Patterns.

UNIT V  SOFTWARE DEVELOPMENT AND APPLICATION  9
Camera with USB port.

TOTAL:  45 PERIODS

COURSE OUTCOMES:
On successful completion of this course, students will be able to
  Make a choice of suitable embedded processor for a given application
• Design the hardware and software for the embedded system
• Design and develop the real time kernel/operating system functions, task control block
  structure and analyze different task states
• Implement different types of inter task communication and synchronization techniques
• To be able to know about the aspects embedded connectivity in real time systems

REFERENCES:
   Design”, Mergen Kaufmann Publisher, 2006.
OBJECTIVES:
To impart knowledge and skills required for research and IPR:
- Problem formulation, analysis and solutions.
- Technical paper writing / presentation without violating professional ethics
- Patent drafting and filing patents.

UNIT I        RESEARCH PROBLEM FORMULATION  6
Meaning of research problem- Sources of research problem, criteria characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations

UNIT II       LITERATURE REVIEW  6
Effective literature studies approaches, analysis, plagiarism, and research ethics.

UNIT III      TECHNICAL WRITING / PRESENTATION  6
Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal, a presentation and assessment by a review committee.

UNIT IV       INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR)  6

UNIT V        INTELLECTUAL PROPERTY RIGHTS (IPR)  6

TOTAL: 30 PERIODS
OUTCOMES:
CO1: Ability to formulate research problem
CO2: Ability to carry out research analysis
CO3: Ability to follow research ethics
CO4: Ability to understand that today’s world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity
CO5: Ability to understand about IPR and filing patents in R & D.

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

REFERENCES:

VE5111 DIGITAL SYSTEM DESIGN LAB

OBJECTIVES:
- To learn Hardware Descriptive Language (Verilog/VHDL)
- To learn the fundamental principles of VLSI circuit design in digital domain
- To familiarize programming on FPGAs
- To understand the critical design issues of digital logic design
- To provide hands on design experience with professional design (EDA) platforms

LIST OF EXPERIMENTS:

Part-I: Module Design using FPGA Implementation (Verilog/VHDL):
1. Adders and Subtractors
2. Multiplier (8-bit)
3. ALU circuit
4. Flip-flops
5. Universal Shift Registers
6. Asynchronous and synchronous Counters
7. Finite State Machine (Moore/Mealy) and its applications
8. Memories

Part-II Module Design using ASIC Implementation (Complete Back-End Design):
1. Adders and Subtractors
2. Multiplier (8-bit)
3. ALU circuit
4. Flip-flops
5. Universal Shift Registers
6. Asynchronous and synchronous Counters
7. Finite State Machine (Moore/Mealy) and its applications
8. Memories

TOTAL: 60 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Write HDL code for basic as well as advanced digital integrated circuit
CO2: Import the logic modules into FPGA Boards
CO3: Synthesize Place and Route the digital ICs
CO4: Design various digital IC blocks
CO5: Design, Simulate and Extract the layouts of Digital ICs

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Write HDL code for basic as well as advanced digital integrated circuit
CO2: Import the logic modules into FPGA Boards
CO3: Synthesize Place and Route the digital ICs
CO4: Design various digital IC blocks
CO5: Design, Simulate and Extract the layouts of Digital ICs

TOTAL: 60 PERIODS

VE5112  EMBEDDED SYSTEMS LABORATORY  L T P C

OBJECTIVES:
- To learn the basic functions of embedded C programming
- To develop the microcontroller programming skills
- To learn about the development tools
- To learn the interfacing techniques of microcontroller
- To design and develop applications related to embedded systems

8-bit/32-bit Microcontroller based Experiments with:

1. Interfacing basic digital input output devices
2. Interfacing a character LCD
3. Interfacing A/D and D/A converter
4. Interfacing Capture/Compare/PWM module
5. DC motor control
6. Multiplexing seven segment LED displays
7. Interfacing Stepper motor and temperature sensor
8. Traffic light controller using IDE

TOTAL: 60 PERIODS
OUTCOMES:
On successful completion of this course, students will be able to
CO1: Write programming to perform microcontroller operation & its interfacing
CO2: Analyze the basic functions of an embedded system
CO3: Analyze the interfacing circuits for embedded systems
CO4: Design a system to meet desired needs of the environment
CO5: To be able to design and develop real time embedded systems

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

VE5201 DESIGN FOR TESTABILITY

OBJECTIVES:
- To describe the various fault models and to understand fault detection
- To understand the difficulties of combinational and sequential circuits under test
- To understand the principles of automatic test pattern generation and testable circuit design
- To understand the built in self-test and boundary scan standard
- To understand the testability techniques for system-on-a-chip design

UNIT - I INTRODUCTION TO TESTING

UNIT - II LOGIC AND FAULT SIMULATION

UNIT – III ATPG FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS
Combinational Circuit: Algorithms and Representations, Redundancy Identification (RID), Combinational ATPG Algorithms - D-Calculus and D-Algorithm, PODEM and FAN.

UNIT – IV DFT METHODS AND BUILT-IN SELF-TEST
DFT Methods - Ad Hoc Approach, Structured Approach - Scan Cell Designs - Scan Architectures - Scan Design Rules - Scan Design Flow.
UNIT – V  BOUNDARY SCAN STANDARD AND CORE-BASED TESTING

Core-Based Design and Test Considerations - Digital Boundary Scan - IEEE Std. 1149.1 - Test Architecture and Operations, Test Access Port and Bus Protocols, Data Registers and Boundary-Scan Cells, TAP Controller - Embedded Core Test Standard (IEEE Std. 1500) - Architecture, Wrapper Components and Functions - Comparisons between 1500 and 1149.1 Standards.

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Design and simulate the fault models
CO2: Apply fault simulation algorithms for circuit under test
CO3: Design test pattern generation circuits for combinational and sequential circuits
CO4: Design built-in self test for circuit under test
CO5: Analyze the testability techniques for Embedded core design

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VE5251 CMOS ANALOG IC DESIGN

OBJECTIVES:
• To learn the equivalent circuits and models of MOS circuits
• To analyze various biasing circuits
• To design and analyze various differential amplifier architectures
• To design and analyze the frequency response of various differential amplifiers
• To discuss the stability and frequency compensation of feedback amplifiers
UNIT - I  SINGLE STAGE AMPLIFIERS
Review of MOS physics and equivalent circuits and models. Large and Small signal analysis CS, CG and source follower, miller effect, frequency response of CS, CG and source follower.

UNIT - II  CURRENT MIRRORS
Current Sources, Basic Current Mirrors, Cascode stages for Current mirrors, Wilson Current Mirror, Widler Current Mirror Large and small signal analysis of current mirrors.

UNIT – III  MULTISTAGE DIFFERENTIAL AMPLIFIERS
Differential amplifier, Large and small signal analysis of the balanced differential amplifier, device mismatches in differential amplifier, small and large signal analysis of the differential pair with current mirror load, PSRR⁺, PSRR⁻ and CMRR of differential amplifiers, small signal analysis of telescopic amplifier, two-stage amplifier and folded cascaded amplifier.

UNIT – IV  FREQUENCY RESPONSE OF MULTISTAGE DIFFERENTIAL AMPLIFIERS
Frequency response of differential amplifier-transfer function method, Miller effect, Dominant-Pole approximation, Upper Cutoff frequency-zero-value time constant method, UGF-short circuit time constant method, frequency response of telescopic cascaded, folded cascaded and two-stage amplifiers.

UNIT – V  STABILITY AND FREQUENCY COMPENSATION OF FEEDBACK AMPLIFIERS
Properties and types of negative feedback circuits, feedback configurations, effect of loading in feedback networks, feedback circuit analysis using return ratio modelling input and output port in feedback network, the relation between gain and bandwidth in feedback amplifiers, phase margin, frequency compensation, compensation of two stage MOS amplifiers.

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze and design CMOS analog IC building blocks
CO2: Design the various current mirror biasing circuits
CO3: Analyze and Design the various single and multistage differential amplifier architectures
CO4: Analyze the frequency response of single and multi-stage differential amplifiers
CO5: Analyze and design various feedback amplifiers with compensation

REFERENCES:
VE5202 HARDWARE - SOFTWARE CO-DESIGN OF EMBEDDED SYSTEM L T P C 3 0 0 3

OBJECTIVES:
- To introduce the key concepts of hardware/software communication
- To learn the data flow implementation in software and hardware
- To learn the concept of integration of custom hardware components with software
- To learn the design space of custom architectures
- To understand the design and implementation experience with case studies

UNIT - I NATURE OF HARDWARE AND SOFTWARE
Hardware, Software, Definition of Hardware/Software Co-Design – Driving factors Platform design space – Application mapping – Dualism of Hardware design and software design – Concurrency and parallelism, Data flow modeling and Transformation – Data Flow Graph – Tokens, actors and queues, Firing rates, firing rules and Schedules – Synchronous data flow graph – control flow modeling – Adding time and resources – Transformations.

UNIT - II DATA FLOW IMPLEMENTATION IN SOFTWARE AND HARDWARE

UNIT – III DESIGN SPACE OF CUSTOM ARCHITECTURES
Finite state machines with datapath – FSMD design example, Limitations – Microprogrammed Architecture – Microprogrammed control, microinstruction encoding, Microprogrammed data path, microprogrammed machine – General purpose Embedded Core – RISC pipeline, Program organization – SoC interfaces for custom hardware – Design Principles in SoC Architecture

UNIT – IV HARDWARE/ SOFTWARE INTERFACES
Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling - On-chip buses – Memory mapped interfaces – coprocessor interfaces – custom instruction interfaces – Coprocessor hardware interface – Data and control design, programmer’s model.

UNIT – V Applications
Zynq processor-centric platforms-Scalable Processor Architecture, Trivium for 8-bit platforms – AES coprocessor, CORDIC coprocessor – algorithm and implementation

TOTAL: 45 PERIODS
OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the key concepts in hardware/software co-design
CO2: Analyze the data flow implementation in software and hardware
CO3: Design the fundamental building blocks using hardware/software co-design and related implementation
CO4: Design and analyze with modern hardware/software tools for building prototypes of embedded systems
CO5: Analyze the various processors

REFERENCES:
5. Louise H. Crockett, “Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC” Strathclyde Academic Media, 2014

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VE5203 EMBEDDED AUTOMATION

OBJECTIVES:
- To learn about the process involved in the design and development of real-time embedded system
- To develop the Embedded C programming skills on 8-bit microcontroller
- To study about the interfacing mechanism of peripheral devices with 8-bit microcontrollers
- To learn about the tools, firmware related to microcontroller programming
- To build a home automation system

UNIT - I INTRODUCTION TO EMBEDDED C PROGRAMMING
C Overview an Program Structure - C types, Operators and Expressions - C control flow - C functions and Program Structures - C pointers and arrays - FIFO and LIFO - C Structures - development tools

UNIT - II AVR MICROCONTROLLER
Atmega16 Architecture - Nonvolatile and Data memories - Port System - Peripheral features : Time base, Timing Subsystem, Pulse width modulation, USART, SPI, Two wire serial Interface, ADC, Interrupts - Physical and operating parameters
UNIT – III HARDWARE AND SOFTWARE INTERFACING WITH 8-BIT SERIES CONTROLLERS

Lights and Switches - Stack operation - Implementing Combinational logic - Expanding I/O - Interfacing Analog to Digital Convertors - Interfacing Digital to Analog Convertors - LED Displays: Seven segment displays, Dot matrix displays - LCD Displays - Driving Relays - Stepper Motor interface - Serial EEPROM - Real Time Clock - Accessing Constants Table - Arbitrary Waveform Generation - Communication links - System Development tools

UNIT – IV VISION SYSTEM


UNIT – V HOME AUTOMATION

Home automation - Requirements - Water level notifier - Electric guard dog - Tweeting bird feeder - Package delivery detector - Web enabled light switch - Curtain automation - Android door lock - Voice controlled home automation - Smart Lighting - Smart Mailbox - Electricity usage monitor - Proximity garage door opener - Vision based authentic entry system

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the 8-bit series microcontroller architecture, features and pin details
CO2: Write Embedded C programs for embedded system application
CO3: Design and develop real time systems using AVR microcontrollers
CO4: Design and develop the systems based on vision mechanism
CO5: Design and develop a real time home automation system

REFERENCES:
VE5211  ANALOG SYSTEM DESIGN LAB

OBJECTIVES:
- To learn the principles of CMOS amplifiers
- To design single stage amplifiers and current mirror circuits
- To understand multistage amplifiers and their design constrains
- To provide hands on design experience with professional design (EDA) platforms
- To design analog hardware blocks using FPAA

LIST OF EXPERIMENTS:

Part I: Module Design and Simulation using Analog Design Environment
1. Design of Common Source Amplifier
2. Design of Cascade and Cascode amplifiers
3. Design of current Mirrors
4. Design of differential pair amplifier with active load
5. Design of telescopic amplifier circuit
6. Design of two-stage amplifier circuit

Part II: Layout extraction and simulation using Analog Design Environment
7. Layout generation, parasitic extraction and layout simulation for experiments 1 to 3.

Part III Analog block hardware design using FPAA
1. Design of variable gain amplifier
2. Filtering Audio signal from noises using notch filter
3. Analyzing frequency response of Band pass filter
4. Monitoring Heart rate signal using PPG sensor

OUTCOMES:
On successful completion of this course, students will be able to
- Design basic and advanced analog circuits
- Design and simulate various amplifiers
- Import the standard cells in analog domain
- Synthesize Place and Route the analog ICs
- Design and analyze various analog blocks using FPAA

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

TOTAL: 60 PERIODS
VE5212  EMBEDDED AUTOMATION LAB  L T P C  0 0 4 2

OBJECTIVES:
- To learn about the design and development of different automation systems
- To enhance the Embedded C programming skills
- To study about the interfacing mechanism of peripheral devices with microcontrollers
- To improve the programming skills related to Computer vision
- To build a home automation system

LIST OF EXPERIMENTS:
1. Water level controller
2. Unauthorized entry identifier
3. Tweeting bird feeder
4. Package delivery detector
5. Web enabled light switch
6. Curtain automation
7. Android door lock
8. Voice controlled home automation
9. Smart Lighting
10. Smart Mailbox
11. Proximity garage door opener

TOTAL: 60 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Design and develop real time systems using microcontrollers
CO2: Design and develop the systems based on vision mechanism
CO3: To be able to build large, complex systems
CO4: Design and develop a real time home automation system
CO5: Students should be able to know the different embedded tools

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VE5001  SOLID STATE DEVICE MODELING  L T P C  3 0 0 3

OBJECTIVES:
- To understand the basic concepts of solid semiconductors
- To understand the principle behind all types of device modeling
- To learn and understand different noise models of devices
- To analyze the device performance in terms of mathematical expressions
- To comprehend the widely used device models in industry such as BSIM and EKV
UNIT - I MOSFET DEVICE PHYSICS
Introduction to solids, Bonding forces and energy bands in solid semiconductors, MOS capacitor - Interface Charge, threshold voltage, MOS Capacitance, MOS Charge control model, MOS Operation and characteristics. MOSFET fabrication process.

UNIT - II MOSFET MODELING

UNIT – III RF AND NOISE MODELING

UNIT – IV BSIM4 MOSFET MODELING
Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, Mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, Noise model, Junction diode models, Layout-dependent parasitics model.

UNIT – V OTHER MOSFET MODELS
The EKV model- model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, temperature effects, MOS model 9, MOSAI model, Influence of process variation, Modeling of device mismatch for Analog/RF Applications.

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the concepts and procedural flow that are used to construct the complicated device models
CO2: Design and analyze different MOSFET models
CO3: Analyze the noise models of MOSFET
CO4: Analyze the design challenges involved in device models
CO5: Analyze the EKV and BSIM4 MOSFET models

REFERENCES:
OBJECTIVES:
- To understand the overview of DSP systems and the concepts of parallel and pipeline techniques
- To acquire knowledge on various retiming algorithms and architectures
- To acquire knowledge on fast convolution algorithms
- To understand the architecture of parallel and pipelined recursive filters
- To develop knowledge on the clocking styles of the digital circuits

UNIT - I  INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING FOR FIR FILTERS  9
Overview of DSP systems – FPGA Technology- DSP Technology Requirements- Data flow and Dependence graphs - Critical path, Loop bound, Iteration bound, Longest path matrix Algorithm, Pipelining and Parallel Processing of FIR filters.

UNIT - II  RETIMING, ALGORITHMIC STRENGTH REDUCTION  9

UNIT – III  FAST CONVOLUTION, PIPELINED AND PARALLEL RECURSIVE AND ADAPTIVE FILTERS  9
Fast convolution – Cook-Toom algorithms, Winograd algorithms, Pipelined and parallel recursive filters – Pipeline Interleaving in Digital Filters - Pipelining in I & II order Digital Filter – Parallel Processing for IIR Filter- Pipelined Adaptive Digital Filters.

UNIT – IV  BIT-LEVEL ARITHMETIC ARCHITECTURES  9
Parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers - Design of Lyon"s bit-serial multipliers using Horner’s rule, Bit-serial FIR filter design - CSD Arithmetic, CSD multiplication using Horner”s rule for precision improvement - Distributed Arithmetic - Offset binary coding.

UNIT – V  NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING  9
Sub-expression Elimination, Multiple Constant Multiplication, Sub-expression sharing - Synchronous pipelining and Clocking styles - Clock skew in edge-triggered single phase clocking and Two-phase clocking - Wave Pipelining - NPCPL - Asynchronous Pipelining.

TOTAL: 45 PERIODS
OUTCOMES:
On successful completion of this course, students will be able to

CO1: Analyze the critical path of the DSP architectures
CO2: Design efficient retiming architecture for FIR filter using data flow graphs
CO3: Analyze various bit-level arithmetic architectures used in signal processing applications
CO4: Design fast convolution algorithms to minimize computational complexity
CO5: Analyze and implement proper clocking techniques on VLSI circuits

REFERENCES:

<table>
<thead>
<tr>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VE5002 VLSI FOR WIRELESS COMMUNICATION

OBJECTIVES:
- To understand the concepts of basic wireless communication systems
- To study the parameters in receiver and low noise amplifier design
- To study the various types of mixers and PLLs design for wireless communication
- To understand the concepts of transmitters and power amplifiers used in wireless communication
- To discuss the architectures of wireless transceivers at the transistor level

UNIT - I COMMUNICATION CONCEPTS

UNIT - II    TRANSMITTER AND RECEIVER ARCHITECTURES 9
Transmitter back end design – Quadrature LO generator, Receiver front end – Filter design – Non-idealities – Design parameters – Noise figure & Input intercept point. LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedance matching & Core amplifier.

UNIT – III    MIXERS 9

UNIT – IV    ANALOG TO DIGITAL CONVERTERS 9
Demodulators – A/D converters used in receivers – Low-pass and band-pass sigma delta modulators and its implementation-I/Q mismatch in converters

UNIT – V    FREQUENCY SYNTHESIZERS 9
PLL – Phase detector – Dividers – Voltage Controlled Oscillators – LC oscillators – Ring Oscillators – Phase noise – Loop filters & design approaches – A complete synthesizer design example (DECT).

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Apply the VLSI concepts in wireless communication techniques
CO2: Design and analyze the LNA and Mixers
CO3: Design and analyze PLL for real time applications
CO4: Analyze the characteristics of receivers and frequency synthesizers
CO5: Design and analyze A/D converters

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent methods.
- Identify suitable techniques to reduce the power dissipation.
- Estimate Power dissipation of various MOS logic circuits.
- Develop algorithms for low power dissipation.

UNIT I  POWER DISSIPATION IN CMOS
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II  POWER OPTIMIZATION
Logic level power optimization – Circuit level low power design – Gate level low power design – Architecture level low power design – VLSI subsystem design of adders, multipliers, PLL, low power design.

UNIT III  DESIGN OF LOW POWER CMOS CIRCUITS
Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – Advanced techniques – Special techniques, Adiabatic techniques – Physical design, Floor planning, placement and routing.

UNIT IV  POWER ESTIMATION
Power Estimation techniques, circuit level, gate level, architecture level, behavioral level, – logic power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V  SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER
Synthesis for low power – Behavioral level transform – Algorithms for low power – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES:
CO1: Ability to find the power dissipation of MOS circuits
CO2: Design and analyse various MOS logic circuits
CO3: Apply low power techniques for low power dissipation
CO4: Able to estimate the power dissipation of ICs
CO5: Ability to develop algorithm to reduce power dissipation by software.

REFERENCES:
OBJECTIVES:
- The course focuses on the semi-custom IC Design and introduces the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles.
- The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I  INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN  9
Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II  PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS  9
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III  PROGRAMMABLE ASIC ARCHITECTURE  9

UNIT IV  LOGIC SYNTHESIS, PLACEMENT AND ROUTING  9

UNIT V  SYSTEM-ON-CHIP DESIGN  9

TOTAL: 45 PERIODS
OUTCOMES:
CO1: Ability to apply logical effort technique for predicting delay, delay minimization and FPGA architectures
CO2: Ability to design logic cells and I/O cells
CO3: Ability to analyze the various resources of recent FPGAs
CO4: Ability to use algorithms for floorplanning and placement of cells and to apply routing algorithms for optimization of length and speed.
CO5: Ability to analyze high performance algorithms available for ASICs

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>3</td>
<td></td>
<td>2</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>3</td>
<td></td>
<td>2</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>3</td>
<td></td>
<td>2</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>3</td>
<td></td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>CO5</td>
<td>3</td>
<td></td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

VE5003 SoC DESIGN FOR EMBEDDED SYSTEM L T P C 3 0 0 3

OBJECTIVES:
- To learn the basics of system-on-chip
- To learn architecture and design concepts underlying system on chips
- To impart knowledge about the hardware-software design of a modest complexity chip all the way from specifications, modeling, synthesis and physical design
- To learn the memory circuits
- To understand various interconnect architectures of SoC design

UNIT - I SYSTEM ARCHITECTURE: OVERVIEW
Components of the system – Processor architectures – Memory and addressing – system level interconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.
UNIT - II  PROCESSOR SELECTION FOR SOC

UNIT – III  MEMORY DESIGN

UNIT – IV  INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION

UNIT – V  FPGA BASED EMBEDDED PROCESSOR

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the components of a System-on-Chip and an embedded system
CO2: Analyze the major design flows for digital hardware and embedded software
CO3: Design and analyze the major architectures and trade-offs of chips and embedded systems
CO4: Design and analyze various interconnect architectures
CO5: Design memory circuits for embedded system applications

REFERENCES:
**OBJECTIVES:**

- To impart knowledge in the concept of a peer to peer interconnection network, shared bus based design, and network on chip (NoC) based architectures
- To address the issues of scalability of on-chip connectivity and inter processor communication
- To introduce the types of networks and performance analysis
- To understand the quality of service provided by NoC
- To analyze various performance metrics of NoC

### UNIT - I INTRODUCTION TO INTERCONNECTION NETWORKS


### UNIT - II TYPES OF NETWORKS

Butterfly Networks, Torus Networks, Mesh Networks, Non-blocking networks, Non-interfacing networks, Crossbar networks, Clos Networks, Beneš Networks, Sorting Networks

### UNIT – III ROUTING & FLOW CONTROL


### UNIT – IV QUALITY OF SERVICE & ROUTER

Guaranteed services, Best-Effort services, Router Datapath Components, Input Buffer organization, Switches, Output Organization, Arbitration, waveform allocator, Processor-Network Interface, Shared-Memory Interface

### UNIT – V PERFORMANCE ANALYSIS


**TOTAL: 45 PERIODS**
OUTCOMES:
On successful completion of this course, students will be able to
CO1: Design various networks by considering design constrains
CO2: Design and Analyze the various types of networks
CO3: Design the routing and flow control in networks
CO4: Analyze the various performance metrics
CO5: Design the quality of service and routing mechanisms

REFERENCES:

<table>
<thead>
<tr>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>☑</td>
<td></td>
<td>☑</td>
<td>✓</td>
<td></td>
<td>•</td>
</tr>
<tr>
<td>☑</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>☑</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>

VE5005 ADVANCED CMOS ANALOG IC DESIGN L T P C
3 0 0 3

OBJECTIVES:
- To understand various sources of noises in Analog Blocks
- To understand various OTA architectures
- To understand the switched-capacitor circuits and data conversion circuits
- To learn and design bandgap reference circuits
- To learn the performance metrics involved in analog IC design

UNIT - I NOISE IN INTEGRATED CIRCUITS
9
Statistical Characteristics of Noise, Sources of noise, noise models of IC components, Circuit noise calculations, equivalent input noise generators, effect of feedback on noise performance, noise in CS, CE, CG and cascode amplifiers, noise in differential pair, noise bandwidth.
UNIT - II OTA DESIGN CONSIDERATION
Step response, Slewing, OTA variations, CMFB implementation, Input resistance, Output resistance, Output Voltage swing, CMRR, PSRR of two-stage telescopic amplifiers.

UNIT – III BANDGAP REFERENCE CIRCUIT AND SWITCHED CAPACITOR CIRCUITS

UNIT – IV PERFORMANCE METRICS OF DATA CONVERTERS & NYQUIST RATE D/A CONVERTERS
Ideal Sampling, Reconstruction, Quantization, Static performance metrics, Dynamic performance metrics, Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs.

UNIT – V ANALOG TO DIGITAL CONVERTERS
Single stage amplifier as comparator, resistor-based latched comparators, offset cancellation, Flash ADC, Successive approximation ADC, Pipelined ADC, Time Interleaved ADC.

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Design various analog block by considering noises and their effects
CO2: Design various OTA architectures and CMFB block
CO3: Design and analyze bandgap reference circuits
CO4: Analyze switched-capacitor circuits and the issue of non-linearity and mismatch in the circuits
CO5: Analyze data conversion circuits such as DAC and ADC and their design techniques.

REFERENCES:

<table>
<thead>
<tr>
<th>CO1</th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TOTAL: 45 PERIODS
OBJECTIVES:

- The student shall develop an overview and deeper insight into the research and development that is underway to meet future needs of flexible processors
- To learn the concepts of implementation, synthesis and placement of modules in reconfigurable architectures
- To understand the communication techniques and system on programmable chip for reconfigurable architectures
- To learn the process of reconfiguration management
- To familiarize the applications of reconfigurable architectures

UNIT - I INTRODUCTION

UNIT - II IMPLEMENTATION, SYNTHESIS AND PLACEMENT

UNIT – III COMMUNICATION AND SoPC

UNIT – IV RECONFIGURATION MANAGEMENT
Reconfiguration – configuration architectures – managing the reconfiguration process – reducing configuration transfer time – configuration security.

UNIT – V APPLICATIONS
FPGA based parallel pattern matching - Low power FPGA based architecture for microphone arrays in wireless sensor networks - Exploiting partial reconfiguration on a dynamic coarse grained reconfigurable architecture – Parallel pipelined OFDM baseband modulator with dynamic frequency scaling for 5G systems.

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the different architecture principles relevant to reconfigurable computing systems
CO2: Compare the tradeoffs that are necessary to meet the area, power and timing criteria of reconfigurable systems
CO3: Analyze the algorithms related to placement and partitioning
CO4: Analyze the communication techniques and system on programmable chip for reconfigurable architectures
CO5: Analyze the principles of network and system on a programmable chip
REFERENCES:

<table>
<thead>
<tr>
<th>CO1</th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✔</td>
<td></td>
<td>✔</td>
<td></td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td>CO5</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✔</td>
</tr>
</tbody>
</table>

VE5006 COMPUTER AIDED DESIGN FOR VLSI SYSTEMS L T P C 3 0 0 3

OBJECTIVES:
- To learn the Algorithmic Graph Theory and computational complexity optimization
- To analyze the concepts of layout design rules and floor planning
- To analyze the algorithms on floor planning and routing
- To learn high level synthesis and scheduling algorithm
- To simulate and synthesis different hardware models

UNIT - I VLSI DESIGN METHODOLOGIES 9
Introduction to VLSI Design methodologies - Review of VLSI Design automation tools – Graph theory and computational complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT - II LAYOUT COMPACTION, PLACEMENT AND PARTITIONING 9

UNIT – III FLOOR PLANNING AND ROUTING 9
Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - Global routing: introduction and algorithms.
UNIT – IV  SIMULATION AND LOGIC SYNTHESIS
Gate level modeling and simulation – Switch level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT – V  HIGH LEVEL SYNTHESIS
Hardware models - Internal representation of input algorithms – Allocation - Assignment - scheduling – scheduling algorithms - assignment problems - high level transformations.

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Implement, simulate and synthesis the computer aided design of VLSI systems
CO2: Analyze the Algorithmic Graph Theory and computational complexity optimization
CO3: Analyze the concepts of layout design rules and floor planning
CO4: Design and optimize circuits using various graphical algorithms
CO5: Simulate and synthesis different hardware models

REFERENCES:

<table>
<thead>
<tr>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

VE5007  DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

OBJECTIVES:
- To understand the architecture and programming of fixed and floating point DSP processors
- To understand the techniques involved in real time DSP system design
- To learn and design the basic forms of FIR and IIR filters
- To understand the fast implementation schemes of DFT
- To understand the structures and algorithms of adaptive filters
UNIT - I  INTRODUCTION TO DIGITAL SIGNAL PROCESSING SYSTEMS  9
Fundamentals of DSP - Digital signal processor architectures – Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.

UNIT - II  FIXED AND FLOATING POINT DIGITAL SIGNAL PROCESSORS  9
TMS320C55x – Architecture overview, Addressing modes, Instruction set, Programming considerations, system issues. TMS320C62x AND TMS320C64x - Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Realtime implementations.

UNIT - III  FAST FOURIER TRANSFORMS  9
Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

UNIT – IV  FIR AND IIR FILTER IMPLEMENTATIONS  9
FIR and IIR filters – Characteristics, Structures, FIR Filter design using Windowing and frequency sampling method, IIR Filter-Butterworth and Chebyshev Filter Design-, Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

UNIT – V  ADAPTIVE FILTER STRUCTURES AND ALGORITHMS  9
Wiener filter, LS filter , Filter structures, Adaptive algorithms, Properties and Applications – Fixed and floating point implementation using TMS320C64x and TMS320C67x.

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Develop the program for fixed and floating point DSP processors based on the design issues
CO2: Design and develop real time implementations on DSP algorithms
CO3: Design IIR and FIR filters with desired frequency responses
CO4: Apply the fast transforms for the analysis of DSP systems
CO5: Analyze the structures and algorithms of adaptive filters

REFERENCES:
5. TMS Manual on TMS320C64XX and TMS320C67XX.
MULTICORE ARCHITECTURES AND PROGRAMMING

**OBJECTIVES:**
- To learn the basics of multicore processing
- To understand the principles of parallel programming
- To understand the principles of different multiprocessors with their performance issues
- To understand the fundamentals of various programming concepts used in multicore architectures
- To learn the concepts of multicore architectures for embedded systems

**UNIT - I**
**INTRODUCTION TO MULTIPROCESSORS AND SCALABILITY ISSUES**
9

**UNIT - II**
**PARALLEL PROGRAMMING**
9

**UNIT – III**
**OPENMP PROGRAMMING**
9

**UNIT – IV**
**MPI PROGRAMMING**
9
MPI Model – collective communication – data decomposition – communicators and topologies – point-to-point communication – MPI Library.

**UNIT – V**
**MULTICORE ARCHITECTURES FOR EMBEDDED SYSTEMS**
9

**TOTAL: 45 PERIODS**
OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the basics of multicore processing
CO2: Analyze the principles of parallel programming
CO3: Analyze the principles of different multiprocessors with their performance issues
CO4: Analyze the fundamentals of various programming concepts used in multicore architectures
CO5: Design the concepts of multicore architectures for embedded systems

REFERENCES:
2. Michael J Quinn, Parallel programming in C with MPI and OpenMP, Tata Mcgraw Hill, 2004.

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

NE5074 IMAGE ANALYSIS AND COMPUTER VISION L T P C 3 0 0 3

OBJECTIVES:
- To introduce to basic concepts and methodologies for digital image processing
- To learn the various image transform techniques
- To understand the general processes of image enhancement, segmentation, representation and description
- To learn the principles of image compression
- To understand the various computer vision based applications
UNIT - I  IMAGE ENHANCEMENT
Digital image fundamentals - Image sampling - Quantization - Spatial domain filtering - intensity transformations - Contrast stretching - Histogram equalization - Smoothing filters, Sharpening filters - Noise distributions - Mean filters - Order statistics filters

UNIT - II  IMAGE TRANSFORMS
1D DFT- 2D Transforms - DFT- DCT- Walsh - Hadamard - Slant - Haar - KLT- SVD- Wavelet transform

UNIT – III  IMAGE RESTORATION AND SEGMENTATION
Image restoration - degradation model - Unconstrained and Constrained restoration - Inverse filtering - Wiener filtering - Image segmentation - Thresholding - Edge detection, Edge linking - Region based methods

UNIT – IV  IMAGE COMPRESSION
Need for data compression - Huffman - Arithmetic coding - LZW technique - Vector Quantization - JPEG – MPEG

UNIT – V  VIDEO PROCESSING
Back ground Subtraction - Video analytics - Video object Segmentation - Object Detection - Face Recognition - Motion Estimation

TOTAL: 45 PERIODS

OUTCOMES:
CO1: To be able to implement image enhancement algorithms
CO2: To be able to apply image transform for different imaging modalities
CO3: To be able to perform different segmentation and restoration processes
CO4: To be able to implement different compression techniques
CO5: To be able to develop algorithms for computer vision problems

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO3</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
OBJECTIVES:

- To familiar with the concepts of quantum logic
- To learn the quantum computing basics and algorithms
- To learn the reversible logic circuits
- To understand various architectural elements and its programming techniques
- To design the sequential circuits using reversible logic gates

UNIT - I QUANTUM COMPUTATIONS AND ALGORITHMS


UNIT – II QUANTUM ARCHITECTURES AND SIMULATION


UNIT – III ARCHITECTURAL ELEMENTS AND PROGRAMMING


UNIT – IV REVERSIBLE LOGIC: FUNDAMENTALS AND SYNTHESIS


UNIT – V REVERSIBLE SEQUENTIAL LOGIC CIRCUITS


TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the basics of quantum computing
CO2: Design and analyze quantum architectures and algorithms
CO3: Design and simulate the basic elements using quantum computing
CO4: Design reversible logic circuits
CO5: Design and analyze sequential circuits using reversible logic

REFERENCES:

OBJECTIVES:

- To understand the basic principles of discrete random signal processing
- To understand the principles of spectral estimation
- To learn about the weiner and adaptive filters
- To understand the different signal detection and estimation methods
- To acquire skills to design synchronization methods for proper functioning of the system

UNIT I DISCRETE RANDOM SIGNAL PROCESSING

UNIT II SPECTRAL ESTIMATION

UNIT III WEINER AND ADAPTIVE FILTERS

UNIT IV DETECTION AND ESTIMATION
Bayes detection techniques, MAP, ML,– detection of M-ary signals, Neyman-Person, minimax decision criteria. kalman filter- Discrete kalman filter, The Extended kalman filter, Application.

UNIT V SYNCHRONIZATION
Signal parameter estimation, carrier phase estimation, symbol timing estimator, joint estimation of carrier phase and symbol timing.

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the basic principles of discrete random signal processing
CO2: Analyze the principles of spectral estimation
CO3: Analyze the weiner and adaptive filters
CO4: Analyze the different signal detection and estimation methods
CO5: Design the synchronization methods for proper functioning of the system
REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NE5078 PATTERN RECOGNITION AND MACHINE LEARNING

OBJECTIVES:
- To understand the basics of data processing and dimensionality reduction techniques
- To understand different learning models for classification
- To understand the principles and applications of ANN architectures
- To study the different Deep convolutional networks
- To learn deep generative models

UNIT - I BASICS OF PROBABILITY AND RANDOM PROCESS
Probability Theory - Conditional and Joint Probability - Stationary and non-stationary process - Expectation - Auto correlation - Cross Correlation - Eigen values - Eigen vectors - Singular values - Singular vectors - Decision Theory - Information Theory

UNIT - II DIMENSIONALITY REDUCTION
Introduction - Features, feature vectors - Feature selection and ranking - Discriminant functions - Fisher’s Discriminant analysis - Principal Component Analysis - Kernel PCA - Independent component analysis

Learning MODELS

UNIT – III
Linear models for Classification and Regression - Classifiers based on Bayes Decision theory – Naïve Bayes - Nearest neighbor rules - Mixture models - Mixture of Gaussian - Hidden Markov Model

UNIT – IV ARTIFICIAL NEURAL NEWORKS
Supervised Learning - Unsupervised Learning - Reinforcement Learning – Feed Forward and Feedback architectures - Multilayer Perceptron - Backpropagation Algorithm - Radial Basis Function networks - Support vector Machines
UNIT – V    DEEP LEARNING NETWORKS


OUTCOMES:
On successful completion of this course, students will be able to
CO1: Employ different feature extraction and dimensionality reduction techniques
CO2: Design different learning models
CO3: Implement different neural network architectures
CO4: Realize basic Deep neural network architectures
CO5: Test and implement deep generative models for various data processing applications

TOTAL: 45 PERIODS

REFERENCES:

<table>
<thead>
<tr>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

VE5010    DISTRIBUTED EMBEDDED COMPUTING  L T P C

OBJECTIVES:
- To learn the fundamentals of Network communication technologies.
- To understand the fundamentals of Internet
- To study on Java based Networking
- To introduce network routing Agents
- To learn the basis for network on-chip technologies

UNIT - I  THE HARDWARE INFRASTRUCTURE

UNIT - II  INTERNET IN EMBEDDED COMPUTING  9
Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT – III  DISTRIBUTED COMPUTING USING JAVA  9

UNIT – IV  EMBEDDED AGENT  9
Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent-Mobile robots.

UNIT – V  EMBEDDED COMPUTING ARCHITECTURE  9

TOTAL:  45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the fundamentals of Network communication technologies
CO2: Analyze the internet and Java based networking
CO3: Design and analyze the network routing agents
CO4: Analyze the various network-on-chip technologies
CO5: Analyze the analog/digital co-design of distributed embedded computing architecture

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
OBJECTIVES:

- To learn the concepts of Serial and parallel communication protocols
- To understand the application development using USB and CAN bus for PIC microcontrollers
- To learn the basics of ethernet
- To learn the application development using embedded internet
- To learn the wireless sensor network communication protocols

UNIT - I  COMMUNICATION PROTOCOLS


UNIT - II  USB AND CAN BUS


UNIT – III  ETHERNET BASICS


UNIT – IV  EMBEDDED ETHERNET

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP.

UNIT – V  EMBEDDED WIRELESS SENSOR NETWORKS

Wireless sensor networks – Introduction to WSN-Challenges for WSNs - Characteristic requirements - Required mechanisms - Single-node architecture - Hardware components - Energy consumption of sensor nodes - Operating systems and execution environments - Some examples of sensor nodes.

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to

CO1: Analyze the wired and wireless network protocols
CO2: Design an application using embedded networking
CO3: Analyze the basics of Ethernet
CO4: Incorporate networks in embedded systems
CO5: Analyze the basics of wireless sensor networks

REFERENCES:


<table>
<thead>
<tr>
<th>CO1</th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>✔</td>
<td></td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
<td>✔</td>
<td></td>
<td></td>
</tr>
<tr>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VE5012 REAL TIME OPERATING SYSTEMS

OBJECTIVES:
- To learn about significance and usage of Real time operating system
- To learn about different scheduling strategies and optimization principles
- To learn about the resource allocation or sharing process involved in RTOS
- To study about the different firmware and tools related to RTOS development
- To design and develop an innovative real time embedded system

UNIT - I REAL TIME EMBEDDED SYSTEMS
Introduction - History of Real time systems and Embedded systems - Real time services and standards - System resources - Analysis - Service utility - Scheduling Classes - Cyclic executive - Scheduler concepts- Real time operating System - Thread safe Reentrant Functions

UNIT - II RESOURCES AND SERVICES
Processing - Resources - Memory - Multiresource services : Blocking, Deadlock, livelock, Critical sections to protect shared resources, Priority inversion, Power management and Processor clock modulation - Soft real time services : Missed deadlines, Quality of Service, Alternatives to Rate monotonic policy, Mixed hard and soft real time services

UNIT – III REAL TIME EMBEDDED COMPONENTS
Hardware components - Firmware components - RTOS system software - Software application components - Traditional Hard real time operating systems : Asymmetric Multicore Processing and Symmetric Multi-core Processing - Processor core affinity - SMP support models - RTOS Hypervisors - Open source real time operating systems

UNIT – IV INTEGRATING EMBEDDED LINUX
Integrating Embedded Linux into Real time systems - Debugging Components - Performance tuning - High availability and Reliability Design - Hierarchical approaches for fail-safe design

UNIT – V CASE STUDIES
System life cycle - Continuous Media applications - video and audio processing - Robotic applications - Computer vision applications

TOTAL: 45 PERIODS
OUTCOMES:
On successful completion of this course, students will be able to
CO1: Complete understanding of scheduling algorithm and process
CO2: Better understanding on firmware and tools related to the development of RTOS
CO3: To be able to design and develop an embedded system with RTOS functionality
CO4: To be able to design and develop the systems in Linux environments
CO5: To be able to develop large real-time embedded systems

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VE5013 EMBEDDED C PROGRAMMING L T P C 3 0 0 3

OBJECTIVES:
- To learn the process involved in the design and development of real-time embedded system
- To develop the programming skills on PIC microcontroller
- To study the interfacing mechanism of peripheral devices with controllers
- To learn the tools, firmware and programming methodologies related to embedded system design
- To improve the knowledge base and programming skill of students in Real time embedded system

UNIT - I INTRODUCTION 9
C Overview an Program Structure - Constants - Preprocessor Directives - Data Variables and Types - Expression and Operators - Statements - Functions - Arrays - Structures - Memory and Pointers - Built in Functions - Strings - Function like Macros - Conditional Compilation
UNIT - II  8-BIT MICROCONTROLLER

UNIT – III  CONFIGURATION AND PROGRAMMING
Minimal Hardware Connection - Device Programming - Hex Files - Power up Considerations - Clock Configuration - Integrated Development Environment -Debugging - Bootloading - Real Time Methods - Using Interrupts - State Machines

UNIT – IV  INTERFACING PERIPHERAL DEVICES

RTOS PROGRAMMING & CASE STUDIES

UNIT – V

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Design a system with embedded C programming and debugging skills
CO2: Interface the peripheral device with microcontroller
CO3: Analyze the scheduling strategies, resource allocation and process methods involved in RTOS
CO4: Design and develop the hardware and software portion in Real-time embedded Systems
CO5: Design and develop innovative real time systems

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>
OBJECTIVES:
- To learn the Fundamentals of Electronic Components related to automotive applications
- To learn on Automotive Sensors, Actuators and Instrumentations
- To learn the Control Mechanisms in an Automotive System
- To learn about the automotive instrumentation system
- To learn Telematics and Diagnostic methods

UNIT - I  SYSTEMS APPROACH TO CONTROL AND INSTRUMENTATION  9

UNIT - II  FUNDAMENTALS OF ELECTRONICS, MICROCOMPUTER INSTRUMENTATION AND CONTROL  9
Semiconductor Devices, Transistors, ICs, Operational Amplifiers, Use of Feedback in Op Amps, Phase-Locked Loop, Digital Circuits, Logic Circuits (Combination and Sequential Circuits), Timers and Counters, Microcomputer fundamentals, Tasks and Operations, CPU Registers, Reading Instructions, Programming Languages, Microcomputer Hardware, Microcomputer Applications in Automotive Systems, Instrumentation Applications of Mirocomputers, Microcomputers in Control Systems.

UNIT – III  SENSORS, ACTUATORS AND ELECTRONIC ENGINE CONTROL  9

UNIT – IV  MOTION AND DIGITAL POWERTRAIN CONTROL SYSTEM  9

UNIT – V  AUTOMOTIVE INSTRUMENTATION, TELEMATICS AND ITS DIAGNOSTICS  9

TOTAL: 45 PERIODS
OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze with the fundamentals of Electronic Components related to automotive applications
CO2: Design Automotive Sensors, Actuators and Instrumentations
CO3: Analyze the Control Mechanisms in an Automotive System
CO4: Analyze the operations of Telematics and Diagnostic methods
CO5: To be able to understand the complete automotive operation and control mechanisms

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✔</td>
<td></td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td></td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td></td>
<td>✔</td>
<td></td>
<td></td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td></td>
<td></td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
</tbody>
</table>

VE5015 MEMS AND MICROSYSTEMS  L T P C  3 0 0 3

OBJECTIVES:
- To understand the fundamentals of MEMS and Microsystems
- To understand the micro mechanism of MEMs
- To learn MEMS accelerometers and actuators design techniques
- To understand the concepts of MEMS interfacing
- To familiarize with some MEMS applications

UNIT - I INTRODUCTION TO MEMS
MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT - II MICROMECHANICS
Elasticity, Stress, strain and material properties, Bending of thin films, Spring configurations, torsion deflection, Mechanical vibration, Resonance, Thermomechanics - actuators, force and response time, Fracture and thin film mechanics.

Page 62 of 84
UNIT – III MICROACTUATORS
Electrostatics: basic theory, electrostatic instability. Surface tension, Gap and finger pull up, Electrostatic actuators, comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators, bistable actuators.

UNIT – IV INTERFACING AND PACKAGING
Electronic Interfaces, Feedback systems, Noise, Packaging: Dicing-Wafer level Packaging-Wafer bonding-Connections between layers-self assembly-higher level of packaging.

UNIT – V CASE STUDIES
Optical MEMS, RF MEMS- System design basics, Case studies: Capacitive accelerometer, Peizo electric pressure sensor, MEMS scanners, Capacitive RF MEMS switch, performance issues.

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the working of MEMS and Microsystems components
CO2: Analyze the principles of micromechanism
CO3: Design and analyze the interfacing of MEMS and microsystems
CO4: Design the MEMS accelerometer and to design Electrostatic actuators
CO5: Analyze the working of RF and Optical MEMS

REFERENCES:

<table>
<thead>
<tr>
<th>CO1</th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>✔</td>
<td></td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td></td>
<td>✔</td>
<td></td>
<td>✔</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✔</td>
<td></td>
<td>✔</td>
<td></td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✔</td>
<td></td>
<td>✔</td>
<td></td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>CO5</td>
<td></td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td>✔</td>
</tr>
</tbody>
</table>

VE5016 RF IC DESIGN

OBJECTIVES:
• To understand the fundamentals of RF integrated circuits operating at microwave frequencies
• To learn the circuit design for low noise amplifiers
• To understand the concepts of power amplifier design
• To learn the fundamentals of PLL and frequency synthesizers
• To learn RFIC design techniques, including system architecture, key building blocks design methodologies in CMOS technology
UNIT - I  COMPONENTS FOR RF IC
MOSFET Physics: Long channel and Short channel approximation, Noise: Two port Noise theory, MOS capacitor, Spiral Inductors, Model for on chip inductors, Bond wire inductors, Monolithic transformer realization, Interconnects.

UNIT - II  CIRCUIT DESIGN FOR LOW NOISE AMPLIFIERS
Methods of Open circuit and Short circuit time constants, Bandwidth enhancers, Tuned amplifier, Neutralisation, cascaded amplifiers, CMOS amplifiers, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT – III   POWER AMPLIFIER DESIGN
Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, Class A, AB, B, C, D, E and F amplifiers, Linearization Techniques, RF power amplifier design example.

UNIT – IV  PLL AND FREQUENCY SYNTHESIZERS
Linearized PLL Model, Noise properties, Phase detectors, Loop filters and Charge pumps, PLL Design examples. Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

UNIT – V  SYSTEM ARCHITECTURE
Receiver architecture: Noise figure, Linearity in cascaded systems, Single and Dual conversion receivers, Image reject receivers, Direct conversion. Transmitter architectures, Detailed Chip design example: WLAN Transceiver architecture.

TOTAL: 45 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the fundamentals of RF integrated circuits operating at microwave frequencies
CO2: Design the circuit for low noise amplifiers
CO3: Design the circuit for power amplifier
CO4: Analyze the fundamentals of PLL and frequency synthesizers
CO5: Analyze RFIC design techniques, including system architecture, key building blocks design methodologies in CMOS technology

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>
OBJECTIVES:
- To get exposed to neural network learning techniques and architectures
- To study fuzzy concepts and models
- To get exposed to hybrid neuro-fuzzy techniques
- To learn the basic concepts in Deep Learning networks
- To understand different optimization techniques and apply the same in different scenarios

UNIT - I NEURAL NETWORKS 9
Biological Neurons Networks - Artificial Neural Networks - Supervised -unsupervised learning - Reinforcement Learning - Activation functions - Perceptrons - Back Propagation networks - Radial Basis Function Networks - Adaptive Resonance architectures - Support Vector Machines

UNIT - II FUZZY LOGIC 9

UNIT – III NEURO - FUZZY MODELING 9

UNIT – IV DEEP LEARNING NETWORKS 9

UNIT – V EVOLUTIONARY ALGORITHMS 9
Heuristic search and optimization techniques -Random search - Introduction to Genetic Algorithms - Social Algorithms

OUTCOMES:
On successful completion of this course, students will be able to
CO1: Design systems based on neural network architectures
CO2: Perform basic operations in fuzzy
CO3: Implement fuzzy models and work on fuzzy tool box
CO4: Design and implement deep learning architectures
CO5: Design optimization based algorithm for a given application

TOTAL: 45 PERIODS

REFERENCES:
OBJECTIVES:

- To learn the fundamentals of robotics
- To learn about the dynamics of robotic controls
- To learn about the navigation mechanisms
- To learn about the hardware and software tools required for building robotic systems
- To learn about different robotic systems

UNIT - I  INTRODUCTION
Introduction, Rigid Transformation, Robot anatomy, Kinematics, Inverse Kinematics, Jacobians, Trajectory Following, Statics and Dynamics.

UNIT - II  ARTIFICIAL LIFE AND ARTIFICIAL INTELLIGENCE

UNIT – III  HARDWARE TOOLS

UNIT – IV  BASIC NAVIGATION

UNIT – V  DESIGN OF ROBOTS
Telepresence robot, Mobile platforms, Walker Robots, Solar-ball Robot, Underwater bots, Aerobots, Robotic arm and IBM PC interface and speech control, Android hand.

TOTAL: 45 PERIODS
OUTCOMES:
On successful completion of this course, students will be able to
CO1: Analyze the dynamics of robotics
CO2: Analyze the hardware and software requirements for robotics
CO3: Build a miniature robotic system
CO4: Design of navigation mechanisms involved in building a robotic system
CO5: To be able to know about different robotic systems

REFERENCES:

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

OE5091 BUSINESS DATA ANALYTICS

OBJECTIVES:
- To understand the basics of business analytics and its life cycle.
- To gain knowledge about fundamental business analytics.
- To learn modeling for uncertainty and statistical inference.
- To understand analytics using Hadoop and Map Reduce frameworks.
- To acquire insight on other analytical frameworks.

UNIT I OVERVIEW OF BUSINESS ANALYTICS
Suggested Activities:
- Case studies on applications involving business analytics.
- Converting real time decision making problems into hypothesis.
- Group discussion on entrepreneurial opportunities in Business Analytics.

Suggested Evaluation Methods:
- Assignment on business scenario and business analytical life cycle process.
- Group presentation on big data applications with societal need.
- Quiz on case studies.

UNIT II  ESSENTIALS OF BUSINESS ANALYTICS
9

Suggested Activities:
- Solve numerical problems on basic statistics.
- Explore chart wizard in MS Excel Case using sample real time data for data visualization.
- Use R tool for data visualization.

Suggested Evaluation Methods:
- Assignment on descriptive analytics using benchmark data.
- Quiz on data visualization for univariate, bivariate data.

UNIT III  MODELING UNCERTAINTY AND STATISTICAL INFERENCE
9

Suggested Activities:
- Solving numerical problems in sampling, probability, probability distributions and hypothesis testing.
- Converting real time decision making problems into hypothesis.

Suggested Evaluation Methods:
- Assignments on hypothesis testing.
- Group presentation on real time applications involving data sampling and hypothesis testing.
- Quizzes on topics like sampling and probability.

UNIT IV  ANALYTICS USING HADOOP AND MAPREDUCE FRAMEWORK
9
Suggested Activities:
- Practical – Install and configure Hadoop.
- Practical – Use web based tools to monitor Hadoop setup.
- Practical – Design and develop MapReduce tasks for word count, searching involving text corpus etc.

Suggested Evaluation Methods:
- Evaluation of the practical implementations.
- Quizzes on topics like HDFS and extensions to MapReduce.

UNIT V OTHER DATA ANALYTICAL FRAMEWORKS

Overview of Application development Languages for Hadoop – PigLatin – Hive – Hive Query Language (HQL) – Introduction to Pentaho, JAQL – Introduction to Apache: Sqoop, Drill and Spark, Cloudera Impala – Introduction to NoSQL Databases – Hbase and MongoDB.

Suggested Activities:
- Practical – Installation of NoSQL database like MongoDB.
- Practical – Demonstration on Sharding in MongoDB.
- Practical – Install and run Pig
- Practical – Write PigLatin scripts to sort, group, join, project, and filter data.
- Design and develop algorithms to be executed in MapReduce involving numerical methods for analytics.

Suggested Evaluation Methods:
- Mini Project (Group) – Real time data collection, saving in NoSQL, implement analytical techniques using Map-Reduce Tasks and Result Projection.

TOTAL: 45 PERIODS

OUTCOMES:
On completion of the course, the student will be able to:
- Identify the real world business problems and model with analytical solutions.
- Solve analytical problem with relevant mathematics background knowledge.
- Convert any real world decision making problem to hypothesis and apply suitable statistical testing.
- Write and Demonstrate simple applications involving analytics using Hadoop and MapReduce
- Use open source frameworks for modeling and storing data.
- Apply suitable visualization technique using R for visualizing voluminous data.

REFERENCES:
OE5092  INDUSTRIAL SAFETY  LT P C  3 0 0 3

OBJECTIVES:
- Summarize basics of industrial safety
- Describe fundamentals of maintenance engineering
- Explain wear and corrosion
- Illustrate fault tracing
- Identify preventive and periodic maintenance

UNIT I  INTRODUCTION
Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT II  FUNDAMENTALS OF MAINTENANCE ENGINEERING
Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT III  WEAR AND CORROSION AND THEIR PREVENTION

UNIT IV  FAULT TRACING
Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, i. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.
UNIT V PERIODIC AND PREVENTIVE MAINTENANCE

Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: i. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

TOTAL: 45 PERIODS

OUTCOMES:
Students will be able to:
CO1: Ability to summarize basics of industrial safety
CO2: Ability to describe fundamentals of maintenance engineering
CO3: Ability to explain wear and corrosion
CO4: Ability to illustrate fault tracing
CO5: Ability to identify preventive and periodic maintenance

<table>
<thead>
<tr>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

REFERENCES:

OE5093 OPERATIONS RESEARCH L T P C
3 0 0 3

OBJECTIVES:
- Solve linear programming problem and solve using graphical method.
- Solve LPP using simplex method
- Solve transportation, assignment problems
- Solve project management problems
- Solve scheduling problems

UNIT I LINEAR PROGRAMMING
Introduction to Operations Research – assumptions of linear programming problems – Formulations of linear programming problem – Graphical method
UNIT II ADVANCES IN LINEAR PROGRAMMING
Solutions to LPP using simplex algorithm - Revised simplex method - primal dual relationships – Dual simplex algorithm - Sensitivity analysis

UNIT III NETWORK ANALYSIS – I
Transportation problems -Northwest corner rule, least cost method, Voges’s approximation method - Assignment problem - Hungarian algorithm

UNIT IV NETWORK ANALYSIS – II
Shortest path problem: Dijkstra’s algorithms, Floyds algorithm, systematic method - CPM/PERT

UNIT V NETWORK ANALYSIS – III
Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models

TOTAL: 45 PERIODS

OUTCOMES:
Students will be able to:
CO1: To formulate linear programming problem and solve using graphical method.
CO2: To solve LPP using simplex method
CO3: To formulate and solve transportation, assignment problems
CO4: To solve project management problems
CO5: To solve scheduling problems

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

REFERENCES:
OBJECTIVES:
- Summarize the costing concepts and their role in decision making
- Infer the project management concepts and their various aspects in selection
- Interpret costing concepts with project execution
- Develop knowledge of costing techniques in service sector and various budgetary control techniques
- Illustrate with quantitative techniques in cost management

UNIT I INTRODUCTION TO COSTING CONCEPTS  
Objectives of a Costing System; Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost; Creation of a Database for operational control.

UNIT II INTRODUCTION TO PROJECT MANAGEMENT  
Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities, Detailed Engineering activities, Pre project execution main clearances and documents, Project team: Role of each member, Importance Project site: Data required with significance, Project contracts.

UNIT III PROJECT EXECUTION AND COSTING CONCEPTS  
Project execution Project cost control, Bar charts and Network diagram, Project commissioning: mechanical and process, Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis, Various decision-making problems, Pricing strategies: Pareto Analysis, Target costing, Life Cycle Costing.

UNIT IV COSTING OF SERVICE SECTOR AND BUDGETERY CONTROL  
Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis, Budgetary Control: Flexible Budgets; Performance budgets; Zero-based budgets.

UNIT V QUANTITATIVE TECHNIQUES FOR COST MANAGEMENT  
Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Learning Curve Theory.

OUTCOMES:
Students will be able to:
- CO1 – Understand the costing concepts and their role in decision making
- CO2 – Understand the project management concepts and their various aspects in selection
- CO3 – Interpret costing concepts with project execution
- CO4 – Gain knowledge of costing techniques in service sector and various budgetary control techniques
- CO5 - Become familiar with quantitative techniques in cost management
<table>
<thead>
<tr>
<th>CO1</th>
<th>CO2</th>
<th>CO3</th>
<th>CO4</th>
<th>CO5</th>
</tr>
</thead>
<tbody>
<tr>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
</tbody>
</table>

REFERENCES:
2. Charles T. Horngren and George Foster, Advanced Management Accounting, 1988

OE5095 COMPOSITE MATERIALS

OBJECTIVES:
- Summarize the characteristics of composite materials and effect of reinforcement in composite materials.
- Identify the various reinforcements used in composite materials.
- Compare the manufacturing process of metal matrix composites.
- Understand the manufacturing processes of polymer matrix composites.
- Analyze the strength of composite materials.

UNIT I INTRODUCTION
Definition – Classification and characteristics of Composite materials - Advantages and application of composites - Functional requirements of reinforcement and matrix - Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT II REINFORCEMENTS
Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers - Properties and applications of whiskers, particle reinforcements - Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures - Isostrain and Isostress conditions.

UNIT III MANUFACTURING OF METAL MATRIX COMPOSITES

UNIT IV MANUFACTURING OF POLYMER MATRIX COMPOSITES
UNIT V  STRENGTH
Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TOTAL: 45 PERIODS

OUTCOMES:
Students will be able to:
- CO1 - Know the characteristics of composite materials and effect of reinforcement in composite materials.
- CO2 – Know the various reinforcements used in composite materials.
- CO3 – Understand the manufacturing processes of metal matrix composites.
- CO4 – Understand the manufacturing processes of polymer matrix composites.
- CO5 – Analyze the strength of composite materials.

<table>
<thead>
<tr>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

REFERENCES:

OE5096  WASTE TO ENERGY

OBJECTIVES:
- Interpret the various types of wastes from which energy can be generated
- Develop knowledge on biomass pyrolysis process and its applications
- Develop knowledge on various types of biomass gasifiers and their operations
- Invent knowledge on biomass combustors and its applications on generating energy
- Summarize the principles of bio-energy systems and their features

UNIT I  INTRODUCTION TO EXTRACTION OF ENERGY FROM WASTE
Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT II  BIOMASS PYROLYSIS
Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.
UNIT III BIOMASS GASIFICATION

UNIT IV BIOMASS COMBUSTION
Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT V BIO ENERGY
Properties of biogas (Calorific value and composition), Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production -Urban waste to energy conversion - Biomass energy programme in India.

TOTAL: 45 PERIODS

OUTCOMES:
Students will be able to:
CO1 – Understand the various types of wastes from which energy can be generated
CO2 – Gain knowledge on biomass pyrolysis process and its applications
CO3 – Develop knowledge on various types of biomass gasifiers and their operations
CO4 – Gain knowledge on biomass combustors and its applications on generating energy
CO5 – Understand the principles of bio-energy systems and their features

<table>
<thead>
<tr>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>

REFERENCES:
**AUDIT COURSES (AC)**

**AX5091 ENGLISH FOR RESEARCH PAPER WRITING**

**OBJECTIVES**
- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

**UNIT I  INTRODUCTION TO RESEARCH PAPER WRITING**
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

**UNIT II  PRESENTATION SKILLS**

**UNIT III  TITLE WRITING SKILLS**
Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

**UNIT IV  RESULT WRITING SKILLS**
Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

**UNIT V  VERIFICATION SKILLS**
Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first-time submission

**TOTAL: 30 PERIODS**

**OUTCOMES**
- **CO1** – Understand that how to improve your writing skills and level of readability
- **CO2** – Learn about what to write in each section
- **CO3** – Understand the skills needed when writing a Title
- **CO4** – Understand the skills needed when writing the Conclusion
- **CO5** – Ensure the good quality of paper at very first-time submission

<table>
<thead>
<tr>
<th>CO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CO2</th>
<th>PO1</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CO3</th>
<th>PO1</th>
<th>PO2</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CO4</th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CO5</th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

Page 77 of 84
REFERENCES

AX5092 DISASTER MANAGEMENT
L T P C
2 0 0 0

OBJECTIVES
- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT I INTRODUCTION
Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II REPERCUSSIONS OF DISASTERS AND HAZARDS

UNIT III DISASTER PRONE AREAS IN INDIA
Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT IV DISASTER PREPAREDNESS AND MANAGEMENT
Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V RISK ASSESSMENT
Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People’s Participation in Risk Assessment. Strategies for Survival

TOTAL : 30 PERIODS
OUTCOMES

CO1: Ability to summarize basics of disaster
CO2: Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
CO3: Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
CO4: Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
CO5: Ability to develop the strengths and weaknesses of disaster management approaches

<table>
<thead>
<tr>
<th></th>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO2</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

REFERENCES

AX5093 SANSKRIT FOR TECHNICAL KNOWLEDGE

OBJECTIVES
- Illustrate the basic sanskrit language.
- Recognize sanskrit, the scientific language in the world.
- Appraise learning of sanskrit to improve brain functioning.
- Relate sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power.
- Extract huge knowledge from ancient literature.

UNIT I ALPHABETS
Alphabets in Sanskrit

UNIT II TENSES AND SENTENCES
Past/Present/Future Tense - Simple Sentences

UNIT III ORDER AND ROOTS
Order - Introduction of roots

UNIT IV SANSKRIT LITERATURE
Technical information about Sanskrit Literature
UNIT V  TECHNICAL CONCEPTS OF ENGINEERING
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TOTAL: 30 PERIODS

OUTCOMES
- CO1 - Understanding basic Sanskrit language.
- CO2 - Write sentences.
- CO3 - Know the order and roots of Sanskrit.
- CO4 - Know about technical information about Sanskrit literature.
- CO5 - Understand the technical concepts of Engineering.

<table>
<thead>
<tr>
<th>PO1</th>
<th>PO2</th>
<th>PO3</th>
<th>PO4</th>
<th>PO5</th>
<th>PO6</th>
<th>PO7</th>
<th>PO8</th>
<th>PO9</th>
<th>PO10</th>
<th>PO11</th>
<th>PO12</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

REFERENCES
1. “Abhyaspustakam” – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. “Teach Yourself Sanskrit” Pramatha Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication

AX5094  VALUE EDUCATION

OBJECTIVES
Students will be able to
- Understand value of education and self-development
- Imbibe good values in students
- Let the should know about the importance of character

UNIT I

UNIT II

UNIT III

UNIT IV

TOTAL: 30 PERIODS
OUTCOMES
Students will be able to
- Knowledge of self-development.
- Learn the importance of Human values.
- Developing the overall personality.

SUGGESTED READING

AX5095 CONSTITUTION OF INDIA L T P C
2000

OBJECTIVES
Students will be able to:
- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals’ constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

UNIT I HISTORY OF MAKING OF THE INDIAN CONSTITUTION:
History, Drafting Committee, (Composition & Working)

UNIT II PHILOSOPHY OF THE INDIAN CONSTITUTION:
Preamble, Salient Features

UNIT III CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES:

UNIT IV ORGANS OF GOVERNANCE:
Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V LOCAL ADMINISTRATION:

UNIT VI ELECTION COMMISSION:
Election Commission: Role and Functioning, Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS
OUTCOMES
Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

SUGGESTED READING
1. The Constitution of India,1950(Bare Act),Government Publication.

AX5096 PEDAGOGY STUDIES

OBJECTIVES
Students will be able to:

- Review existing evidence on there view topic to inform programme design and policy
- Making under taken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

UNIT I INTRODUCTION AND METHODOLOGY:
Aims and rationale, Policy background, Conceptual framework and terminology - Theories of learning, Curriculum, Teacher education - Conceptual framework, Research questions - Overview of methodology and Searching.

UNIT II THEMATIC OVERVIEW
Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries - Curriculum, Teacher education.

UNIT III EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES
Methodology for the in depth stage: quality assessment of included studies - How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? - Theory of change - Strength and nature of the body of evidence for effective pedagogical practices - Pedagogic theory and pedagogical approaches - Teachers’ attitudes and beliefs and Pedagogic strategies.
UNIT IV PROFESSIONAL DEVELOPMENT
Professional development: alignment with classroom practices and follow up support - Peer support - Support from the head teacher and the community - Curriculum and assessment - Barriers to learning: limited resources and large class sizes

UNIT V RESEARCH GAPS AND FUTURE DIRECTIONS
Research design – Contexts – Pedagogy - Teacher education - Curriculum and assessment - Dissemination and research impact.

TOTAL: 30 PERIODS

OUTCOMES
Students will be able to understand:

- What pedagogical practices are being used by teachers informal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

SUGGESTED READING

AX5097 STRESS MANAGEMENT BY YOGA L T P C
2 0 0 0

OBJECTIVES
- To achieve overall health of body and mind
- To overcome stress

UNIT I
Definitions of Eight parts of yoga.(Ashtanga)

UNIT II
Yam and Niyam - Do’s and Don’t’s in life - i) Ahinsa, satya, astheya, bramhacharya and aparigraha, ii) Ahinsa, satya, astheya, bramhacharya and aparigraha.
UNIT III
Asan and Pranayam - Various yog poses and their benefits for mind & body - Regularization of breathing techniques and its effects - Types of pranayam

TOTAL: 30 PERIODS

OUTCOMES
Students will be able to:
- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

SUGGESTED READING
1. ‘Yogic Asanas for Group Training Part-I” : Janardan Swami Yoga bhyasi Mandal, Nagpur
2. “Rajayoga or conquering the Internal Nature” by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

AX5098 PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS L T P C
TOTAL: 30 PERIODS

OBJECTIVES
- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

UNIT I
Neetisatakam-holistic development of personality - Verses- 19, 20, 21, 22 (wisdom) - Verses- 29, 31, 32 (pride & heroism) – Verses- 26, 28, 63, 65 (virtue) - Verses- 52, 53, 59 (don’ts) - Verses- 71, 73, 75, 78 (do’s)

UNIT II
Approach to day to day work and duties - Shrimad Bhagwad Geeta: Chapter 2- Verses 41, 47, 48 - Chapter 3- Verses 13, 21, 27, 35 Chapter 6- Verses 5, 13, 17, 23, 35 - Chapter 18- Verses 45, 46, 48.

UNIT III
Statements of basic knowledge - Shrimad Bhagwad Geeta: Chapter 2- Verses 56, 62, 68 Chapter 12 - Verses 13, 14, 15, 16, 17, 18 - Personality of role model - shrimad bhagwad geeta - Chapter 2- Verses 17, Chapter 3- Verses 36, 37, 42 - Chapter 4- Verses 18, 38, 39 Chapter 18 - Verses 37, 38, 63

SUGGESTED READING
1. Gopinath, Rashtriya Sanskrit Sansthanam P, Bhartrihari’s Three Satakam, Niti-sringar-vairagya, New Delhi, 2010