ANNA UNIVERSITY, CHENNAI
NON - AUTONOMOUS COLLEGES AFFILIATED ANNA UNIVERSITY
M.E. VLSI DESIGN AND EMBEDDED SYSTEMS
REGULATIONS – 2021
CHOICE BASED CREDIT SYSTEM

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):

1. To enrich students in the cutting edge technologies of VLSI design and Embedded systems and create competent professionals and researchers in this field
2. To provide students with a good foundation in computer architecture principles and digital systems design as these areas are vital for the VLSI design industry
3. To understand the various applications and employ embedded systems to find solutions to them with good scientific and engineering knowledge so as to comprehend, analyze, design, and create novel products and solutions for the real life problems.
4. To provide students with an academic environment aware of excellence, leadership, ethical conduct, positive attitude, societal responsibilities and the lifelong learning needed for a successful professional career.
5. To inculcate entrepreneurial skills in setting startups serving the needs of the industry sectors that depend on VLSI design and Embedded Systems.

PROGRAM SPECIFIC OUTCOMES (PSOs):

At the end of this program, the students will be able to

1. Master the fundamentals, associated with the different specializations of VLSI and Embedded systems domain.
2. Provide solutions through research to the social relevant issues with the knowledge, techniques, skills in VLSI and Embedded systems domain using the required hardware and modern tools for the benefit of the society.
3. Pursue a successful research career in VLSI and Embedded systems field or take on challenging assignments in the industry.

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I TO IV SEMESTERS CURRICULA AND SYLLABI
SEMESTER I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL4153	Graph Theory and Optimization Techniques	FC	3	1	0	4	4
2.	RM4151	Research Methodology and IPR	RMC	2	0	0	2	2
3.	VL4151	Analog IC Design	PCC	3	0	0	3	3
4.	VL4152	Digital CMOS VLSI Design	PCC	3	0	0	3	3
5.	VE4151	Embedded Controllers	PCC	3	0	0	3	3
6.	VE4152	Embedded System Design	PCC	3	0	0	3	3
7.		Audit Course – I*	AC	2	0	0	2	0
PRACTICALS								
8.	VE4111	Embedded Systems Laboratory	PCC	0	0	4	4	2
9.	VE4112	Analog and Digital CMOS VLSI Design Laboratory	PCC	0	0	4	4	2
			TOTAL	**19**	**1**	**8**	**28**	**22**

*Audit course is optional

SEMESTER II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL4251	Design for Verification using UVM	PCC	3	0	0	3	3
2.	VE4201	FPGA System Design	PCC	3	0	2	5	4
3.	VE4202	Embedded Automation	PCC	3	0	0	3	3
4.	VE4203	VLSI Structures for DSP	PCC	3	0	0	3	3
5.	VE4204	Internet of Things System Design	PCC	3	0	0	3	3
6.		Professional Elective I	PEC	3	0	0	3	3
7.		Audit Course – II*	AC	2	0	0	2	0
PRACTICALS								
8.	VE4211	Term Paper and Seminar	EEC	0	0	2	2	1
9.	VE4212	Embedded Automation Laboratory	PCC	0	0	4	4	2
			TOTAL	**20**	**0**	**8**	**28**	**22**

*Audit course is optional

SEMESTER III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.		Professional Elective II	PEC	3	0	0	3	3
2.		Professional Elective III	PEC	3	0	0	3	3
3.		Professional Elective IV	PEC	3	0	2	5	4
4.		Open Elective	OEC	3	0	0	3	3
PRACTICALS								
5.	VE4311	Project Work I	EEC	0	0	12	12	6
			TOTAL	**12**	**0**	**14**	**26**	**19**

SEMESTER IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICALS								
1.	VE4411	Project Work II	EEC	0	0	24	24	12
			TOTAL	**0**	**0**	**24**	**24**	**12**

TOTAL NO. OF CREDITS: 75

PROFESSIONAL ELECTIVES

SEMESTER II, ELECTIVE I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4071	ASIC Design	PEC	3	0	0	3	3
2.	VE4001	Parallel and Reconfigurable Architectures	PEC	3	0	0	3	3
3.	VE4002	Software for Embedded Systems	PEC	3	0	0	3	3
4.	VE4003	Embedded System Security	PEC	3	0	0	3	3
5.	VL4254	VLSI Testing	PEC	3	0	0	3	3
6.	VL4074	Network on Chip	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4075	Nanotechnology	PEC	3	0	0	3	3
2.	VL4252	Low Power VLSI Design	PEC	3	0	0	3	3
3.	VE4004	Multicore Architecture Programming	PEC	3	0	0	3	3
4.	VE4005	Reconfigurable Computing	PEC	3	0	0	3	3
5.	VE4071	Hardware Software Co-Design	PEC	3	0	0	3	3
6.	II4072	System on Chip	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4073	MEMS and NEMS	PEC	3	0	0	3	3
2.	AP4071	Automotive Electronics	PEC	3	0	0	3	3
3.	VE4006	Embedded Wireless Sensor Networks	PEC	3	0	0	3	3
4.	VE4007	Network Embedded Applications	PEC	3	0	0	3	3
5.	VL4253	RFIC Design	PEC	3	0	0	3	3
6.	AP4077	Sensors and Actuators	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VE4008	Real Time Operating System	PEC	3	0	2	5	4
2.	VE4009	Embedded Networking	PEC	3	0	2	5	4
3.	IF4073	Deep Learning	PEC	3	0	2	5	4
4.	VE4072	Real Time Embedded Systems	PEC	3	0	2	5	4
5.	VE4010	Pervasive Computing	PEC	3	0	2	5	4
6.	VE4011	Physical Design Automation	PEC	3	0	2	5	4

AUDIT COURSES (AC)

Registration for any of these courses is optional to students

SL. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS
			L	T	P	
1.	AX4091	English for Research Paper Writing	2	0	0	0
2.	AX4092	Disaster Management	2	0	0	0
3.	AX4093	Constitution of India	2	0	0	0
4.	AX4094	நற்றமிழ் இலக்கியம்	2	0	0	0

FOUNDATION COURSES (FC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	VL4153	Graph Theory and Optimization Techniques	3	1	0	4	I

PROFESSIONAL CORE COURSES (PCC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	VL4151	Analog IC Design	3	0	0	3	I
2.	VL4152	Digital CMOS VLSI Design	3	0	0	3	I
3.	VE4151	Embedded Controllers	3	0	0	3	I
4.	VE4152	Embedded System Design	3	0	0	3	I

5.	VE4111	Embedded Systems Laboratory	0	0	4	2	I
6.	VE4112	Analog and Digital CMOS VLSI Design Laboratory	0	0	4	2	I
7.	VL4251	Design for Verification using UVM	3	0	0	3	I I
8.	VE4201	FPGA System Design	3	0	2	4	I I
9.	VE4202	Embedded Automation	3	0	0	3	I I
10.	VE4203	VLSI Structures for DSP	3	0	0	3	I I
11.	VE4204	Internet of Things System Design	3	0	0	3	I I
12.	VE4212	Embedded Automation Laboratory	0	0	4	2	I I
					TOTAL CREDITS		

RESEARCH METHODOLOGY AND IPR COURSES (RMC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	RM4151	Research Methodology and IPR	2	0	0	2	1
					TOTAL CREDITS	2	

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	VE4211	Mini Project with	0	0	2	1	III
2.	VE4311	Project Work I	0	0	12	6	III
3.	VE4411	Project Work II	0	0	24	12	IV
					TOTAL CREDITS		

SUMMARY

Sl. No.	Name of the Programme:					
	SUBJECT AREA	CREDITS PER SEMESTER				CREDITS TOTAL
		I	II	III	IV	
1.	FC	04	00	00	00	04
2.	PCC	16	18	00	00	33
3.	PEC	00	03	10	00	13

4.	RMC	02	00	00	00	02
5.	OEC	00	00	03	00	03
6.	EEC	00	01	06	12	19
7.	Non Credit/Audit Course	✓	✓	00	00	
8.	**TOTAL CREDIT**	**22**	**22**	**19**	**12**	**75**

VL4153 GRAPH THEORY AND OPTIMIZATION TECHNIQUES L T P C
3 1 0 4

COURSE OBJECTIVES:

- To introduce graph as mathematical model to solve connectivity related problems.
- To introduce fundamental graph algorithms.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in real life situation.
- To provide knowledge and training using non-linear programming under limited resources for the engineering and business problems.
- To understand the applications of simulation modelling in engineering problems.

UNIT I GRAPHS 12

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

UNIT II GRAPH ALGORITHM 12

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

UNIT III LINEAR PROGRAMMING 12

Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.

UNIT IV NON-LINEAR PROGRAMMING 12

Constrained Problems – Equality constraints – Lagrangean Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.

UNIT V SIMULATION MODELLING 12

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems.

TOTAL : 60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

1. apply graph ideas is solving connectivity related problems.
2. apply fundamental graph algorithms to solve certain optimization problems.
3. formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
4. model various real life situations as optimization problems and effect their solution through Non-linear programming.
5. apply simulation modeling techniques to problems drawn from industry management and other engineering fields.

REFERENCES:

1. Taha H.A, “Operation Research: An Introduction”, Ninth Edition, Pearson Education, New Delhi, 2010.

2. Gupta P. K, and Hira D.S., “Operation Research”, Revise Edition, S. Chand and Company Ltd., 2012.
3. Sharma J.K., “Operation Research”, 3rd Edition, Macmillan Publishers India Ltd., 2009.
4. Douglas B. West, “Introduction to Graph Theory”, Pearson Education, New Delhi, 2015.
5. Balakrishna R., Ranganathan. K., “ A text book of Graph Theory”, Springer Science and Business Media, New Delhi, 2012.
6. Narasingh Deo, “Graph Theory with Applications to Engineering and Computer Science”, Prentice Hall India,1997.

RM4151 **RESEARCH METHODOLOGY AND IPR** **L T P C**
2 0 0 2

UNIT I RESEARCH DESIGN **6**

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

UNIT II DATA COLLECTION AND SOURCES **6**

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.

UNIT III DATA ANALYSIS AND REPORTING **6**

Overview of Multivariate analysis, Hypotheses testing and Measures of Association.
Presenting Insights and findings using written reports and oral presentation.

UNIT IV INTELLECTUAL PROPERTY RIGHTS **6**

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT V PATENTS **6**

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.

TOTAL:30 PERIODS

REFERENCES:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education, 11e (2012).
2. Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007.
3. David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
4. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.

VL4151 **ANALOG IC DESIGN** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- Analog Circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology. The most important building blocks of all CMOS analog IC will be the topic of study in this course.
- The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.
- The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.

UNIT I SINGLE STAGE AMPLIFIERS **9**

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

UNIT II HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS **9**

Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.

UNIT III FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS **9**

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER **9**

Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage And Using Cascode Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, And Compensation Of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.

UNIT V BANDGAP REFERENCES **9**

Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascode current source, design of high swing cascode sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing.

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Design amplifiers to meet user specifications 9
CO2: Analyse the frequency and noise performance of amplifiers
CO3: Design and analyse feedback amplifiers and one stage op amps
CO4: Design and analyse two stage op amps
CO5: Design and analyse current mirrors and current sinks with mos devices

TOTAL: 45 PERIODS

REFERENCES:

1. Behzad Razavi, “Design Of Analog Cmos Integrated Circuits”, Tata Mcgraw Hill, 2001.
2. Willey M.C. Sansen, “Analog Design Essentials”, Springer, 2006.
3. Grebene, “Bipolar And Mos Analog Integrated Circuit Design”, John Wiley & Sons,Inc.,2003.
4. Phillip E.Allen, Douglas R .Holberg, “Cmos Analog Circuit Design”, Oxford University Press, 2nd Edition, 2002.
5. Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320_2021/start
6. Jacob Baker “CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3rd Edition, 2010.

VL4152	DIGITAL CMOS VLSI DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To introduce the transistor level design of all digital building blocks common to all cmos microprocessors, network processors, digital backend of all wireless systems etc.
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, elmore constant , CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS 9

Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.

UNIT V MEMORY ARCHITECTURES 6

Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Use mathematical methods and circuit analysis models in analysis of CMOS digital circuits

CO2: Create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort

CO3: Design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches

CO4: Understand design methodology of arithmetic building blocks

CO5: Design functional units including ROM and SRAM

TOTAL PERIODS:45

REFERENCES:

1. N.Weste, K. Eshraghian, " Principles Of Cmos VLSI Design", Addision Wesley, 2nd Edition, 1993
2. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
3. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design", Mcgraw-Hill, 1998
4. Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective", Prentice Hall Of India, 2nd Edition, Feb 2003

VE4151 EMBEDDED CONTROLLERS L T P C

3 0 0 3

COURSE OBJECTIVES:

- To study the architecture and programming of PIC microcontrollers.
- To learn interfacing with PIC microcontrollers.
- To understand the ARM processor architecture.
- To program using ARM Instruction Set.
- To design and develop embedded applications.

UNIT I PIC MICROCONTROLLER – ARCHITECTURE 9

RISC Vs CISC Architectures – PIC Architecture and Assembly Language Programming - Program Memory Organization- Branch, Call and Time Delay Loop - PIC I/O Port Programming - Arithmetic and Logic Instructions and Programs - PIC Bank Switching, Table Processing, Macros And Modules PIC Configuration Registers-PIC Hardware Connection-ROM Loaders.

UNIT II PIC INTERFACING 9

PIC Timer / Counter Programming - Timers 0 And 1- Programming Timers 2 and 3 -Serial Port Programming -Interrupt Programming -Flash / EEPROM Programming - Standard and Enhanced CCP Modules -Compare Mode Programming - Capture Mode Programming- PWM Programming- ECCP Programming.

UNIT III ARM ARCHITECTURE 9

Introduction to ARM Processor families – Pipeline- ARM7TDMI Programmers Model- Processor Modes-Program Status Registers - Vector Table- Assembler Rules and Directives - Predefined Register Names – Macros – Assembler – Operators – Literals - Load and Store Instructions - Operand Addressing – Endianness - Arm Rotation Scheme - Loading Constants and Addresses into Registers.

UNIT IV ARM PROGRAMMING 9

ARM Instruction Set - Data Processing Instructions – Branch Instructions -– Load Store Instructions – Software Interrupt Instruction – Program Status Register Instructions – Conditional Execution - Thumb Instruction Set-Thumb Programmers Model-Thumb Branch Instructions- Thumb Data Processing Instructions-Thumb Single Register Data Transfer- Thumb Multiple Register Data Transfer Instructions - Thumb Implementation.

UNIT V EMBEDDED APPLICATIONS 9

ADC, DAC and Sensor Interfacing –LCD and Keyboard Interfacing -Calculator with Keypad – Relays and Optoisolators - Stepper Motor Interfacing - DC Motor Interfacing - PWM Motor Control with CCPDC - Motor Control With ECCP.

SUGGESTED ACTIVITIES:

1: Interfacing PIC microcontrollers with peripherals.
2: Assignments on programming ARM processors.
3: Design embedded systems for real – time applications.

COURSE OUTCOMES:

CO1: Understand the architecture of a PIC microcontroller.
CO2: Program using PIC microcontrollers.
CO3: Program using ARM processors.
CO4: Design interfacing circuits with PIC microcontrollers.
CO5: Design embedded applications to solve real world problems.

TOTAL PERIODS:45

REFERENCES:

1. Muhammad Ali Mazidi, "PIC Microcontrollers and Embedded Systems using Assembly and C for PIC18 ", Pearson Education, 2016.
2. William Hohl, "ARM Assembly Language", CRC Press, Second Edition, 2015.
3. John B. Peatman, "Design with PIC Microcontrollers", Pearson Education, Singapore – 1998
4. Andrew Sloss, Dominic Symes, and Chris Wright, "ARM System Developer's Guide Designing and Optimizing System", The Morgan Kaufmann Series, 2004.
5. Steve Furber,"ARM System-on-Chip Architecture", Addison- Wesley Professional; ll Edition 2000.

VE4152 EMBEDDED SYSTEM DESIGN L T P C

3 0 0 3

COURSE OBJECTIVES:

- To understand the design challenges in embedded systems.
- To program the Application Specific Instruction Set Processors.
- To understand the bus structures and protocols.
- To model processes using a state – machine model.
- To design a real time embedded system.

UNIT I EMBEDDED SYSTEM OVERVIEW 9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Components, Optimizing Custom Single-Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR 9

Basic Architecture, Pipelining, Superscalar and VLIW Architectures, Programmer's View, Development Environment, Application-Specific Instruction-Set Processors (ASIPS) Microcontrollers, Timers, Counters and Watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES **9**

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus - based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM bus, Wireless Protocols – IRDA, Bluetooth, IEEE 802.11.

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS **9**

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, RTOS – System design using RTOS.

UNIT V SYSTEM DESIGN **9**

Burglar alarm system-Design goals -Development strategy-Software development-Relevance to more complex designs- Need for emulation -Digital echo unit-Creating echo and reverb-Design requirements-Designing the codecs -The overall system design

SUGGESTED ACTIVITIES:

1: Do microcontroller based design experiments.
2: Create program –state models for different embedded applications.
3: Design and develop embedded solutions for real world problems.

COURSE OUTCOMES:

CO1: Knowledge of different protocols
CO2: Apply state machine techniques and design process models.
CO3: Apply knowledge of embedded sotware development tools and RTOS
CO4: Apply networking principles in embedded devices.
CO5: Design suitable embedded systems for real world applications.

TOTAL:45 PERIODS

REFERENCES:

1. Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & Sons, 2009.
2. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.
3. Bruce Powel Douglas, “Real Time UML, Second Edition: Developing Efficient Objects for Embedded Systems”, 3rd Edition 2004, Pearson Education
4. Daniel W.Lewis, “Fundamentals of Embedded Software where C and Assembly Meet”, Pearson Education, 2004
5. Bruce Powel Douglas, “Real Time UML; Second Edition: Developing Efficient Objects for Embedded Systems”, 3rd Edition 1999, Pearson Education.

VE4111 EMBEDDED SYSTEMS LABORATORY **L T P C**
0 0 4 2

COURSE OBJECTIVES:

- To interface sensors and display devices with microcontroller.
- To program timers and UART in a microcontroller.
- To understand I2C and CAN protocols.
- To understand concepts of scheduling, semaphores and deadlocks using RTOS.
- To design a real – time data acquisition system.

LIST OF EXPERIMENTS:

1: Interfacing sensors and actuators with microcontroller.
2**:** Configuration and programming timers and UART in microcontroller.
3: Interfacing LCD and OLED display modules with microcontroller.
4: Simulation of I2C and CAN protocols.
5: Simple task scheduling using freeware RTOS.
6: Exploration on semaphores, deadlocks using RTOS.
7: Exploration of any one SOC architecture using RTOS.
8: Study of Edge AI platform on any one of the embedded processors.
9: Design of a real – time data acquisition system and control using a microcontroller.
10. Design of an IoT based system.

HARDWARE/SOFTWARE REQUIREMENTS

1: Any microcontroller
2: RTOS Freeware

COURSE OUTCOMES:

CO1: Interface a microcontroller with input – output devices.
CO2: Understand I2C and CAN protocols.
CO3: Explore concepts in RTOS.
CO4: Design a real – time embedded system.
CO5: Analyse design requirements of an IoT based system.

TOTAL:60 PERIODS

REFERENCES

1. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & Sons, 2009.
2. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.
3. Bruce Powel Douglas, "Real Time UML, Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 2004, Pearson Education
4. Daniel W.Lewis, "Fundamentals of Embedded Software where C and Assembly Meet", Pearson Education, 2004
5. Bruce Powel Douglas, "Real Time UML; Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 1999, Pearson Education.

VE4112	**ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY**	**L T P C**
		0 0 4 2

COURSE OBJECTIVES:

- To learn the principles of CMOS amplifiers
- To design single stage and multistage amplifiers and their design constrains
- To learn Hardware Descriptive Language(Verilog/VHDL)
- To learn the fundamental principles of VLSI circuit design in digital domain
- To familiarize programming on FPGAs
- To understand the critical design issues of digital logic design

LIST OF EXPERIMENTS:

Part I: Module Design and Simulation using SPICE simulator

1. Design of Common Source Amplifier
2. Design of Cascade and Cascode amplifiers
3. Design of current Mirrors
4. Design of differential pair amplifier with active load
5. Design of telescopic amplifier circuit
6. Design of two-stage amplifier circuit

Part Ii: Module Design using FPGA Implementation (Verilog/VHDL):

1. Adders and Subtractors
2. Multiplier (8-bit)
3. ALU circuit
4. Flip-flops
5. Universal Shift Registers
6. Asynchronous and synchronous Counters
7. Finite State Machine (Moore/Mealy) and its applications
8. Memories

TOTAL: 60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design digital and analog Circuit using CMOS given a design specification.

CO2: Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances

CO3: Use EDA tools for Circuit Design

VL4251	DESIGN FOR VERIFICATION USING UVM	L T P C 3 0 0 3

OBJECTIVES:

- To provide the students complete understanding on UVM testing
- To become proficient at UVM verification,
- To provide an experience on self checking UVM testbenches

UNIT I INTRODUCTION 9

Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation

UNIT II DEVELOPING REUSABLE VERIFICATION COMPONENTS 9

Modeling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage

UNIT III UVM USING VERIFICATION COMPONENTS 9

Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes - Verification Component Configuration - Creating and Selecting a User-Defined Test - Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards- Implementing a Coverage Model

UNIT IV UVM USING THE REGISTER LAYER CLASSES 9

Using The Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register-Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre-Defined Sequences

UNIT V ASSIGNMENT IN TESTBENCHES 9

Assignment, APB: Protocol, Test bench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, students will be able to

1. understand the basic concepts of two methodologies UVM
2. build actual verification components.
3. generate the register layer classes.
4. code testbenches using UVM.
5. understand advanced peripheral bus testbenches.

REFERENCES

1. https://www.udemy.com/learn-ovm-UVM/ 2.

2. http://www.testbench.in/ut_00_index.html 3.

3. http://www.testbench.in/ot_00_index.html

4. https://www.accellera.org/images/downloads/standards/UVM/UVM_users_guide_1.2.pdf

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	0	3	3	1	0
CO2	3	0	3	3	2	0
CO3	3	0	3	3	2	0
CO4	3	0	3	3	2	0
CO5	3	0	3	3	2	0
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(9/4)=2.5	(0/0)=0

VE4201	FPGA SYSTEM DESIGN	L T P C 3 0 2 4

OBJECTIVES:

1. Students can understand the concepts of FPGA and the need for FPGA in embedded.
2. the course is to provide a thorough understanding about and hands-on practice with FPGA based digital system design and emulation
3. To make the student learn, FPGA fundamentals, design and implementation of Circuits In Them
4. Understanding the Role of FPGAs and ASIC In Embedded Systems

UNIT I FPGA ARCHITECTURE AND OVERVIEW 9

Embedded System Design Flow - Robot Control System - Digital Design Platforms - Microprocessor Based Design - Single-Chip Computer/Microcontroller-Based Design - Application Specific Standard Products (ASSPs) - Design Using FPGA - Robotic Rover Application - FPGA Devices - FPGA and CPLD – Architecture of a Spartan-3 ETM FPGA - Floor Plan and Routing - Timing Model for a FPGA - FPGA Power Usage.

UNIT II EMBEDDED SYSTEM DESIGN 9

FPGA-Based Embedded Processor - Design Re-Use Using On-Chip Bus Interface - Creating a Customized Microcontroller - Robot Axis Position Control - FPGA-Based Signal Interfacing And Conditioning – Motor Control Using FPGA- Case Studies for Motor Control -Prototype using FPGA- FPGA Design Test Methodology

UNIT III VERILOG CONSTRUCTS 9

VLSI Design Flow- Behavioral Style, the Dataflow Style, And Structural Style - Data Types - Constants - Assignment Statement - Operators - Conditional Expressions – Statement Types - Vector Operations – Bit Selects - Functions - Gate Level Modeling

UNIT IV VERILOG MODELING COMBINATIONAL CIRCUITS 9

Combinational Logic -Adders - Multiplexers - Decoders -Comparator -Parity Generators ALU – Three State Gate - UART Model.

UNIT V VERILOG MODELLING SEQUENTIAL CIRCUITS 9

Modelling Latches and Flip Flops-- Sequential Logic - Memory - Registers-Counters Modeling FSM Design Synchronous And Asynchronous - Shift Register- Test Bench Verification. Stepper Motor Control, Servo Motor Control.

TOTAL:45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1. Design Entry Using VHDL Or Verilog Using HDL Languages of

I. Combinational Circuits Namely 8:1 Mux/Demux, Full Adder, 8-Bit Magnitude Comparator, Encoder/Decoder, Priority Encoder.

Ii. Sequential Circuits Namely D-FF, 4-Bit Shift Registers (SISO, SIPO, PISO, Bidirectional), 3-Bit Synchronous Counters.

2. Test Vector Generation And Timing Analysis of Sequential And Combinational Logic Design for exercise (1) above.
3. Synthesis, P&R And Post P&R Simulation of the Components Simulated In (1) Above.
4. FPGA Implementation of PCI Bus & Arbiter. .
5. Verifying Design Functionality Using Either Chipscope Feature (Xilinx) /the Signal Tap Feature (Altera)/Other Equivalent Feature . Invoke the PLL And Demonstrate the Use of the PLL Module for Clock Generation in FPGAs.

OUTCOMES:

CO1: students can learn the concepts of FPGA.
CO2: students can design embedded system with appropriate FPGA based on applications
CO3: students can write verilog code for combinational and sequential logics
CO4: students can design a combinational circuit using Verilog.
CO5: students can use FPGA EDA tools for design and analysis.

REFERENCES

1. Rahul Dubey, "Introduction to Embedded System Design Using Field Programmable Gate Arrays" Springer-Verlag London Limited, 2009
2. John F. Wakerly, Digital Design Principles And Practices", Pearson Education, Asia, Iii Edition, 2003.
3. Blaine Readler, "Verilog By Example: a Concise Introduction for FPGA Design", Full ARC Press,2011.
4. J. Bhasker, "a Verilog HDL Primer, Third Edition Hardcover", Star Galaxy Publishing; 3rd Edition, 2005
5. J.Bhasker, "Verilog HDL Synthesis, a Practical Primer", Star Galaxy Publishing; 3rd Edition,1998.

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	0	3	3	0	0
CO2	3	0	3	3	3	1
CO3	3	1	3	3	3	1
CO4	3	1	3	3	3	1
CO5	3	0	3	3	3	1
AVG	(15/5)=3	(2/2)=1	(15/5)=3	(15/5)=3	(12/4)=3	(4/4)=1

VE4202	EMBEDDED AUTOMATION	L T P C 3 0 0 3

OBJECTIVES:

1. To learn about the process involved in the design and development of real-time embedded system
2. To develop the embedded C programming skills on 8-bit microcontroller
3. To study about the interfacing mechanism of peripheral devices with 8-bit microcontrollers
4. To learn about the tools, firmware related to microcontroller programming
5. To build a home automation system

UNIT - I INTRODUCTION TO EMBEDDED C PROGRAMMING 9

C Overview and Program Structure - C Types, Operators and Expressions - C Control Flow - C Functions and Program Structures - C Pointers And Arrays - FIFO and LIFO - C Structures - Development Tools

UNIT - II AVR MICROCONTROLLER 9

ATMEGA 16 Architecture - Nonvolatile and Data Memories - Port System - Peripheral Features : Time Base, Timing Subsystem, Pulse Width Modulation, USART, SPI, Two Wire Serial Interface, ADC, Interrupts - Physical and Operating Parameters

UNIT – III HARDWARE AND SOFTWARE INTERFACING WITH 8-BIT SERIES CONTROLLERS 9

Lights and Switches - Stack Operation - Implementing Combinational Logic - Expanding I/O - Interfacing Analog To Digital Convertors - Interfacing Digital To Analog Convertors - LED Displays : Seven Segment Displays, Dot Matrix Displays - LCD Displays - Driving Relays - Stepper Motor Interface - Serial EEPROM - Real Time Clock - Accessing Constants Table - Arbitrary Waveform Generation - Communication Links - System Development Tools

UNIT – IV VISION SYSTEM 9

Fundamentals of Image Processing - Filtering - Morphological Operations - Feature Detection and Matching - Blurring and Sharpening - Segmentation - Thresholding - Contours - Advanced Contour Properties - Gradient - Canny Edge Detector - Object Detection - Background Subtraction

UNIT – V HOME AUTOMATION 9

Home Automation - Requirements - Water Level Notifier - Electric Guard Dog - Tweeting Bird Feeder - Package Delivery Detector - Web Enabled Light Switch - Curtain Automation - Android Door Lock - Voice Controlled Home Automation - Smart Lighting - Smart Mailbox - Electricity Usage Monitor -Proximity Garage Door Opener - Vision Based Authentic Entry System

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to
CO1: analyze the 8-bit series microcontroller architecture, features and pin details
CO2: write embedded C programs for embedded system application
CO3: design and develop real time systems using AVR microcontrollers
CO4: design and develop the systems based on vision mechanism
CO5: design and develop a real time home automation system

REFERENCES:

1. Dhananjay V. Gadre, "Programming and Customizing the AVR Microcontroller", McGraw-Hill, 2001.
2. Joe Pardue, "C Programming for Microcontrollers ", Smiley Micros, 2005.
3. Steven F. Barrett, Daniel J. Pack, "ATMEL AVR Microcontroller Primer : Programming and Interfacing", Morgan & Claypool Publishers, 2012
4. Mike Riley, "Programming Your Home - Automate With Arduino, Android and Your Computer", the Pragmatic Programmers, Llc, 2012.
5. Richard Szeliski, "Computer Vision: Algorithms and Applications", Springer, 2011.
6. Kevin P. Murphy, "Machine Learning - a Probabilistic Perspective", the MIT Press Cambridge, Massachusetts, London, 2012.

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3		3	3	3	
CO2	3	1	3	3	3	1
CO3	3	1	3	3	3	1
CO4	3	1	3	3	3	1
CO5	3	1	3	3	3	1
AVG	(15/5)=3	(4/4)=1	(15/5)=3	(15/5)=3	(15/5)=3	(4/4)=1

VE4203 **VLSI STRUCTURES FOR DSP** **L T P C**
3 0 0 3

OBJECTIVES:

1: To Understand the Fundamentals of DSP
2: To Learn Various DSP Structures And Their Implementation.
3: To Know Designing Constraints of Various Filters
4: Design And Optimize VLSI Architectures for Basic DSP Algorithms
5: To Enable Students To Design VLSI System With High Speed And Low Power.

UNIT I INTRODUCTION TO DIGITAL SIGNAL PROCESSING 9

Linear System Theory- Convolution- Correlation - DFT- FFT- Basic Concepts In FIR Filters And IIR Filters- Filter Realizations. Representation of DSP Algorithms-Block Diagram-SFG-DFG.

UNIT II ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER 9

Data-Flow Graph Representations- Loop Bound and Iteration Bound Algorithms for Computing Iteration Bound-LPM Algorithm. Pipelining and Parallel Processing: Pipelining of FIR Digital Filters

UNIT III RETIMING, UNFOLDING AND FOLDING 9

Retiming: Definitions Properties and Problems- Solving Systems of Inequalities. Properties of Unfolding, Critical Path, Unfolding and Retiming Applications of Unfolding, Folding Transformation- Register Minimization Techniques, Register Minimization In Folded Architecture- Folding of Multirate System.

UNIT IV FAST CONVOLUTION 9

Cook-Toom Algorithm- Modified Cook-Toom Algorithm. Design of Fast Convolution Algorithm By Inspection

UNIT V ARITHMETIC STRENGTH REDUCTION IN FILTERS 9

Parallel FIR Filters-Fast FIR Algorithms-Two Parallel And Three Parallel. Parallel Architectures for Rank Order Filters -Odd Even Merge Sort Architecture-Rank Order Filter Architecture-Parallel Rank Order Filters-Running Order, Merge Order , Sorter , Low Power Rank Order Filter.

TOTAL:45 PERIODS

OUTCOMES:

At the end of the course student will be able
CO1: acquired knowledge about fundamentals of DSP processors.
CO2: improve the overall performance of DSP system through various transformation and optimization techniques.
CO3: foster ability to understand the need of different types of instructions for DSP.
CO4: optimize design in terms of computation complexity and speed.
CO5: understand clock based issues and design asynchronous and wave pipelined systems**.**

REFERENCES

1. K.K Parhi: “VLSI Digital Signal Processing”, John-Wiley, 2nd Edition Reprint, 2008.
2. John G.Proakis, Dimitris G.Manolakis, “Digital Signal Processing”, Prentice Hall of India, 1st Edition, 2009.

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	0	3	3	0	0
CO2	3	0	3	3	0	0
CO3	3	0	3	3	0	0
CO4	3	0	3	3	0	0
CO5	3	0	3	3	0	0
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(0/0)=0	(0/0)=0

VE4204	**INTERNET OF THINGS SYSTEM DESIGN**	**L T P C 3 0 0 3**

OBJECTIVES:

1. the course enables student to understand the basics of Internet of Things and protocols
2. This program aims to train students to be equipped with a solid theoretical foundation, systematic professional knowledge and strong practical skills in the IoT platform and system design.
3. the course focuses on understanding the vision of IoT from a global perspective, understand its applications, determine its market perspective, using gateways, devices and data management
4. To understand the concepts behind building a state of art architecture in IoT.
5. the course focuses on applications in commercial building automation and real world design constraints

UNIT I	**IOT NETWORKING CORE**	**9**

Technologies Involved In IoT Development, Internet Web And Networking Technologies, Infrastructure, Overview of IoT Supported Hardware Platforms Such As: Raspberry Pi, ARM Cortex Processors, Arduino and Intel Galileo Boards, Wireless Networking Equipment and Configurations, Accessing Hardware and Device File Interactions

UNIT II	**M2M TO IOT**	**9**

Role of M2M In IoT, M2M Value Chains, IoT Value Chains, An Emerging Industrial Structure for IoT, the International Driven Global Value Chain And Global Information Monopolies. Building Architecture, Main Design Principles and Needed Capabilities, An IoT Architecture Outline, Standards Considerations.

UNIT III	**IOT ARCHITECTURE -STATE OF THE ART**	**9**

IoT Reference Model And Architecture- Functional View, Information View, Deployment and Operational View, Other Relevant Architectural Views, Middleware Introduction-Fiware etc., Remote Monitoring and Sensing, Remote Controlling And Performance Analysis, Layering Concepts, Communication Pattern, 6LoWPAN, Sensors And Sensor Node And Interfacing Using any Embedded Target Boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino

UNIT IV	**IOT APPLICATION DEVELOPMENT**	**9**

Application Protocols: MQTT, Rest/Http, COAP, MYSQL, Back-End Application Designing Apache for Handling Http Requests, MONGODB Object Type Database, HTML, CSS & JQUERY for UI Designing, JSON Lib for Data Processing, Security & Privacy During Development

UNIT V	**IOT SECURITY AND CASE STUDIES**	**9**

Security, Privacy and Trust in IoT-Data-Platforms for Smart Cities, First Steps Towards a Secure Platform, Smartie Approach. Data Aggregation for the IoT in Smart Cities.

TOTAL:45 PERIODS

OUTCOMES

At the end of this course, the students should will be able to:

CO1:study of basic structure lying in IoT
Coy2: understand challenges in Internet of Things (IoT) system design
CO3: understand distributed embedded system hardware.
CO4: understand specifications and modeling approaches for real-time and IoT systems
CO5: obtain knowledge of IoT applications

TOTAL PERIODS:45

REFERENCES

1. Vijay Madisetti and Arshdeepbahga, “Internet of Things (a Hands-On-Approach)”, 1 St Edition, Vpt, 2015

2. Adrian Mcewen, Hakim Cassimally, “Designing the Internet of Things”, November 2013, John Wiley And Sons.

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	0	3	3	0	0
CO2	3	0	3	3	0	0

CO3	3	0	3	3	0	0
CO4	3	0	3	3	0	0
CO5	3	0	3	3	0	0
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(0/0)=0	(0/0)=0

VE4211 **TERM PAPER WRITING AND SEMINAR** **L T P C**
0 0 2 1

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (atleast 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing each paper.
6. Preparing a working outline
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.
Activities to be carried out

Activity	Instructions	Submission week	Evaluation
Selection of area of interest and Topic Stating an Objective	You are requested to select an area of interest, topic and state an objective	2nd week	**3 %** Based on clarity of thought, current relevance and clarity in writing
Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society 2. List 2 journals 3. List 2 conferences, symposia or workshops 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularly in your area 7. Attach a call for papers (CFP) from your area.	3rd week	**3%** (the selected information must be area specific and of international and national standard)

Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter	• You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar • When picking papers to read - try to: • Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, • Favour papers from well-known journals and conferences, • Favour "first" or "foundational" papers in the field (as indicated in other people's survey paper), • Favour more recent papers, • Pick a recent survey of the field so you can quickly gain an overview, • Find relationships with respect to each other and to your topic area (classification scheme/categorization) • Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered	4th week	**6%** (the list of standard papers and reason for selection)
Reading and notes for first 5 papers	Reading Paper Process • For each paper form a Table answering the following questions: • What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • How does the work build on other's work, in the author's opinion? • What simplifying assumptions does the author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)	5th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for next5 papers	Repeat Reading Paper Process	6th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based

			on your conclusions about each paper)
Reading and notes for final 5 papers	Repeat Reading Paper Process	7th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	**8%** (this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	**6%** (Clarity, purpose and conclusion) **6%** Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	**5%** (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11thweek	**10%** (this component will be evaluated based on the linking and classification among the papers)
Your conclusions	Write your conclusions and future work	12th week	**5%** (conclusions – clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th week	**10%** (formatting, English, Clarity and linking) **4%** Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th & 15th week	**10%** (based on presentation and Viva-voce)

TOTAL: 30 PERIODS

VE4212 **EMBEDDED AUTOMATION LAB** **L T P C**
0 0 4 2

OBJECTIVES:

- To learn about the design and development of different automation systems
- To enhance the embedded C programming skills
- To study about the interfacing mechanism of peripheral devices with microcontrollers
- To improve the programming skills related to computer vision
- To build a home automation system

LIST OF EXPERIMENTS:

1. Water level controller
2. Unauthorized entry identifier
3. Tweeting bird feeder
4. Package delivery detector
5. Web enabled light switch
6. Curtain automation
7. Android door lock
8. Voice controlled home automation
9. Smart lighting
10. Smart mailbox
11. Proximity garage door opener
12. **Wi Fi Managed Vehicle Parking and Theft Control**

TOTAL: 60 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to
CO1: design and develop real time systems using microcontrollers
CO2: design and develop the systems based on vision mechanism
CO3: to be able to build large, complex systems
CO4: design and develop a real time home automation system
CO5: students should be able to know the different embedded tools

	1	2	3	4	5	6
CO1	3	3	3	3	3	1
CO2	3	3	3	3	3	1
CO3	3	3	3	3	3	1
CO4	3	3	3	3	3	1
CO5	3	3	3	3	3	1
AVG	(15/5)=3	(15/5)=3	(15/5)=3	(15/5)=3	(15/5)=3	(5/5)=1

VL4071 **ASIC DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

1. To Focus on the Semi-Custom IC Design and introduces the Principles of Design Logic Cells, I/O Cells and Interconnect Architecture, with Equal Importance given to FPGA and ASIC styles.
2. To deal with the entire FPGA and ASIC Design Flow from the Circuit and Layout Design Point of View

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of Asics - Design Flow - CMOS Transistors - Combinational Logic Cell – Sequential Logic Cell - Data Path Logic Cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical Effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti Fuse - Static Ram - EPROM and EEPROM Technology - ACTEL ACT- Xilinx LCA –ALTERA FLEX - ALTERA MAX DC & AC Inputs and Outputs - Clock & Power Inputs - Xilinx I/O Blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECTURE 9

Architecture and Configuration of ARTIX / Cyclone and KINTEX Ultra Scale / STRATIX FPGA – Micro-Blaze / NIOS Based Embedded Systems – Signal Probing Techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING 9

Logic Synthesis - Floor Planning Goals and Objectives, Measurement of Delay in Floor Planning, Floor Planning Tools, I/O and Power Planning, Clock Planning, Placement Algorithms. Routing: Global Routing, Detailed Routing, Special Routing.

UNIT V SYSTEM-ON-CHIP DESIGN 9

SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators. Case Studies: Digital Camera, SDRAM, High Speed Data standards.

TOTAL :45 PERIODS

OUTCOMES:

At the end of this course, the students will be

CO1: able to apply Logical Effort Technique for predicting Delay, Delay Minimization and FPGA Architectures

CO2: able to Design Logic Cells and I/O Cells

CO3: able to analyze the various resources of recent FPGAs

CO4: able to use Algorithms for Floor Planning and Placement of Cells and to Apply Routing Algorithms for Optimization of Length and Speed.

CO5: able to analyze High Performance Algorithms Available for ASICs

REFERENCES

1. M.J.S.Smith, "Application Specific Integrated Circuits", Pearson, 2003.
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science,2006
3. Roger Woods, John Mcallister, Dr. Ying Yi, Gaye Lightbod, “FPGA-Based Implementation of Signal Processing Systems”, Wiley, 2008.

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	0	3	2	1	0
CO2	3	0	3	2	1	0
CO3	3	0	3	2	1	0
CO4	3	0	3	2	1	0
CO5	3	0	3	2	1	0
Avg	(15/5)=3	(0/0)=0	(15/5)=3	(10/5)=2	(5/5)=1	(0/0)=0

VE4001 PARALLEL AND RECONFIGURABLE ARCHITECTURES **L T P C 3 0 0 3**

1. To Educate the Students to the Fundamentals of Parallel Processing
2. To Teach the Fundamentals of Network Topologies for Multiprocessors
3. To Introduce Different Pipeline Designs
4. To Introduce Features of Parallel Processors , Memory Technologies, OS for Multi-programmed Computer
5. To Involve Discussions/ Practice/Exercise Onto Revising & Familiarizing the Concepts Acquired Over the 5 Units of the Subject for Improved Employability Skills

UNIT - I THEORY OF PARALLELISM 9

Parallel Computer Models – the State of Computing-Introduction to Parallel Processing-Parallelism in Uniprocessor & Multiprocessors, Parallel Architectural Classification Schemes-Speedup Performance Laws- -Program and Network Properties-H/W-S/W Parallelism.

UNIT - II SYSTEM INTERCONNECT ARCHITECTURES 9

Integration – FPGA Design Flow – Logic Synthesis – LUT Based Technology Mapping – Modeling – Temporal Partitioning Algorithms – Offline and Online Temporal Placement – Managing Device's Free and Occupied Spaces.

UNIT – III PIPELINING AND SUPERSCALAR TECHNOLOGIES 9

Pipeline Principle and Implementation-Classification of Pipeline Processor - Introduction of Arithmetic, Instruction, Processor Pipelining-Pipeline Mechanisms-Hazards.

UNIT – IV HARDWARE TECHNOLOGIES 9

Introduction to Features of Advanced Embedded Processors through basic comparative study: of Architectures -Addressing Modes -Instruction Types performance of- Parallel and Scalable Architectures, Multiprocessor and SIMD, MIMD Computers, RISC, CISC, Superscalar, VLIW , Vector, Systolic Processors of their unique features -scalable, Multithreaded and Dataflow Architectures inter PE Communication-Interconnection Networks- Array & Vector Processors, Vector Instruction Types Performance Modeling-Design of Vectorising Compiler- Case Architecture of Itanium Processor, Pentium Processor, SPARC Processor

UNIT – V OS ISSUES FOR MULTI PROCESSOR 9

Introduction-Need for Preemptive OS – Synchronising and Scheduling in Multiprocessor OS-, usual OS Scheduling Techniques, Threads – Classification of Multiprocessor OS – Software Requirements of Multiprocessor OS, Distributed Scheduler – PVM – PT Threads in Shared Memory Systems.

TOTAL:45 PERIODS

OUTCOMES:

At the end of this course, the students will be

CO1: Able to understand the operations of Multiprocessor and Multicomputer Systems.

CO2: Able to understand the various Advanced Processor Technology, Pipelining and Scalable Architectures.

CO3: Able to know the working of Superscalar Pipeline, Cache Memory Organization.

CO4: Able to understand the principles of Multithreading, Multi Thread Architecture, Static and Dynamic Dataflow.

CO5: To improve employability and entrepreneurship capacity due to knowledge upgradation on recent trends in Embedded Systems Design.

REFERENCES

1. Kai Hwang “Advanced Computer Architecture”.Tata Mcgraw Hill
2. Rajiv Chopra, ‘Advanced Computer Architecture” S Chand , 2010
3. John L. Hennessy, David A. Petterson, “Computer Architecture: A Quantitative Approach”, 4thedition, Elsevier, 2007
4. Dezsosima, Terence Fountain, Peter Kacsuk, “Advanced Computer Architecture – A Designspace Approach”. Pearson Education,2003.
5. Sajjan G. Shiva “Advanced Computer Architecture”, Taylor & Francis, 2008

	1	2	3	4	5	6
CO1	3	0	3	3	0	0
CO2	3	0	3	3	0	0
CO3	3	0	3	3	0	0

CO4	3	0	3	3	0	0
CO5	3	0	3	3	0	0
Avg	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(0/0)=0	(0/0)=0

VE4002 SOFTWARE FOR EMBEDDED SYSTEMS L T P C
3 0 0 3

Objectives:

1. To Expose the Students to the fundamentals of Embedded Programming
2. To introduce the GNU C Programming Tool Chain in Linux.
3. To study the basic Concepts of Embedded C.
4. To teach the basics of Python Programming
5. To involve Discussions/ Practice/Exercise onto Revising & familiarizing the concepts acquired over the 5 units of the subject for Improved Employability Skills.

UNIT I BASIC C PROGRAMMING 9

Typical C Program Development Environment - Introduction to C Programming – Structured Program Development in C - Data Types and Operators - C Program Control - C Functions - Introduction to Arrays.

UNIT II EMBEDDED C 9

Adding Structure to 'C' Code: Object Oriented Programming with C, Header Files for Project and Port, Examples. Meeting Real-Time Constraints: Creating Hardware Delays - Need for Timeout Mechanism - Creating Loop Timeouts - Creating Hardware Timeouts.

UNIT III C PROGRAMMING TOOL-CHAIN IN LINUX 9

C Preprocessor - Stages of Compilation - Introduction to GCC - Debugging with GDB - the Make Utility - GNU Configure and Build System - GNU Binary Utilities - Profiling - Using GPROF - Introduction to GNU C Library.

UNIT IV PYTHON PROGRAMMING 9

Introduction - Parts of Python Programming Language - Control Flow Statements - Functions - Strings - Lists - Dictionaries - Tuples and Sets.

UNIT V MODULES, PACKAGES AND LIBRARIES IN PYTHON 9

Python Modules and Packages - Creating Modules and Packages - Practical Example – Libraries for Python - Library for Mathematical Functionalities and Tools - Numerical Plotting Library – GUI Libraries for Python - Imaging Libraries for Python – Networking Libraries.

TOTAL:45 PERIODS

OUTCOMES:

At the end of this course, the students will be

CO1: able to understand C Programming and its Salient Features for Embedded Systems

CO2: able to learning Process Delivers Insight Into Various Programming Languages/Software Compatible to Embedded Process Development with Improved Design & Programming Skills.

CO3: able to develop knowledge on C Programming in Linux environment.

CO4: able to write Python Programming for Embedded applications.

CO5: able to improve Employability and Entrepreneurship Capacity due to knowledge upgradation on recent trends in Embedded Programming Skills.

REFERENCES

1. Paul Deitel and Harvey Deitel, “C How to Program”, 8th Edition, Pearson Education Limited, 2016.
2. Michael J Pont, "Embedded C", Addison-Wesley, An Imprint of Pearson Education, 2002.
3. William Von Hagen, "the Definitive Guide to GCC", 2nd Edition, Apress Inc., 2006.
4. Gowrishankar S and Veena A, "Introduction to Python Programming", CRC Press, Taylor & Francis Group, 2019
5. John Paul Mueller, "Beginning Programming with Python for Dummies", 2nd Edition, John Wiley & Sons Inc., 2018.

	1	2	3	4	5	6
CO1	3	0	3	3	1	0
CO2	3	0	3	3	2	0
CO3	3	0	3	3	2	0
CO4	3	0	3	3	2	0
CO5	3	0	3	3	2	1
Avg	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(9/5)=1.8	(1/1)=1

VE4003 **EMBEDDED SYSTEM SECURITY** **L T P C**
3 0 0 3

Objectives:

1. To introduce Embedded Security issue. Security Major Concerns Data, Design and System Protection.
2. To learn Cryptographic Concepts in the Context of Embedded Systems and their Unique Constraints and Requirements.
3. To expose Forensics Procedures and Digital Data Acquisition Mechanisms using FKT and FRED

UNIT I INTRODUCTION 9

the CIA Triad, Identification, Authentication and Authorization, Security Principles and Models. Network Attacks - Types and Sources, Architecture Security, Secure Network Design, Firewalls, Introduction to Intrusion Controls (IDS/IPS), Introduction to Wireless LAN Security Standards, the One-Time Pad, Cryptographic Modes, Block Ciphers, Authenticated Encryption, Public Key Cryptography, Key Agreement, Public Key Authentication

UNIT II EMBEDDED CRYPTOGRAPHY 9

Elliptic Curve Cryptography, Cryptographic Hashes, Message Authentication Codes, Random Number Generation, Key Management for Embedded Systems, Cryptographic Certifications. Introduction to Data Protection Protocols for Embedded Systems. Internet Security for Embedded Systems, IPsec., **Data at-Rest Protocols.**

UNIT III EMBEDDED SYSTEMS SECURITY REQUIREMENTS AND ISSUES 9

Embedded System Security Requirements and Issues, Embedded Software Attacks and Countermeasures, Hardware Security in Embedded Systems, Secured Hardware Architectures for Embedded Systems, Tamper- Resistant Hardware, Introduction to Trust Models for Secure Embedded Hardware and Software Embedded Processing Architectures for Security, Communications Security in Embedded Systems.

UNIT IV DIGITAL FORENSICS 9

The Six A's, Forensic Types: Disk Forensics, Network Forensics, Mobile Device Forensics, Live Forensics, Memory Forensics, Multimedia Forensics, Internet Forensics, Cyber Crime Investigations and Digital Forensics, Disk Based Forensics, Cybercrime, Forensic Process and Methodology, Digital Evidence, Incident Response, Searching and Analysis Tools, Email & Browsers, Intrusion Detection, Attack Trace-Back, Packet Inspection, Log Analysis, Hashing Issues, Anti-Forensics (Encryption and Stealth Techniques), Forensics in Embedded Systems.

UNIT V PRACTICE WITH FORENSIC TOOLS 9

Data Acquisition Hardware Tools, Use Fred to Create Images on Different Media, Recovering the Deleted Files, Investigative Tools (Open Source and Proprietary), Using Forensic Software Such as FTK/Encase Etc. Use FTK Preview Evidence, Export Evidence Files, Create Forensic Images and Convert Existing Images, Create a Case in FTK, Use FTK to Process and Analyze Documents, Metadata, Graphics and E-Mail, Use the FTK Data Carving Feature to Recover Files from Unallocated Disk Space. Web/E-Mail Forensics analysis, Mobile Evidence, Extracting and Analysing Mobile Evidence.

TOTAL:45 PERIODS

OUTCOMES:

At the end of the course, students will demonstrate the ability to:

1. Recognize vulnerabilities, attacks and need of protection mechanisms for embedded systems
2. Analyze and evaluate software vulnerabilities and attacks on Operating Systems
3. Identify terms/concepts relevant to Embedded Cryptography.
4. Develop and deploy solutions for Security of Embedded Software and Data Protection.

TOTAL PERIODS:45

REFERENCES

1. David Kleidermacher, Mike Kleidermacher, Embedded Systems Security - Practical Methods for Safe and Secure Software and Systems Development, Newnes, Elsevier, 2012.
2. Charlie Kaufman, Radia Perlman, and Mike Speciner, Network Security: Private Communication in a Public World, Prentice Hall.
3. Francine Krief (Editor), Communicating Embedded Systems: Networks Applications, Wiley.
4. John Sammons, Digital Forensics with the Access data Forensic Toolkit (FTK), McGraw Hill Companies
5. CEH: Certified Ethical Hacker Version 8 Study Guide By Sean-Philip Oriyano (Author) Publisher Sybex

	1	2	3	4	5	6
CO1	3	0	2	2	3	0
CO2	3	0	2	2	3	0

CO3	3	0	2	2	3	0
CO4	3	0	3	2	3	0
AVG	(12/4)=3	0	(9/4)=2.4	(8/4)=2	(12/4)=3	0

VL4254 **VLSI TESTING** **L T P C**
3 0 0 3

OBJECTIVES:

1. to introduce the VLSI testing.
2. to introduce logic and fault simulation and testability measures
3. to study the test generation for combinational and sequential circuits
4. to study the design for testability.
5. to study the fault diagnosis

UNIT I INTRODUCTION TO TESTING 9

Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing - Test Economics and Product Quality – Fault Modeling – Relationship Among Fault Models.

UNIT II LOGIC & FAULT SIMULATION & TESTABILITY MEASURES 9

Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – Scoap Controllability and Observability

UNIT III TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG

UNIT IV DESIGN FOR TESTABILITY 9

Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Built-in Self-Test – Random Logic Bist – DFT for Other Test Objectives.

UNIT V FAULT DIAGNOSIS 9

Introduction and Basic Definitions – Fault Models for Diagnosis – Generation of Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.

TOTAL:45 PERIODS

OUTCOMES:

At the end of this course, the students should will be able to:

1. Understand VLSI Testing Process
2. Develop Logic Simulation and Fault Simulation
3. Develop Test for Combinational and Sequential Circuits
4. Understand the Design for Testability
5. Perform Fault Diagnosis.

REFERENCES

1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, “VLSI Test Principles and Architectures”, Elsevier, 2017

2. Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits” , Kluwer Academic Publishers, 2017.

3. Niraj K. Jha and Sandeep Gupta, “Testing of Digital Systems”, Cambridge University Press, 2017.

VL4074 NETWORK ON CHIP **L T P C 3 0 0 3**

OBJECTIVES:

The students should be made to:

1. Understand the concept of Network - on - Chip
2. Learn router architecture designs
3. Study fault tolerance Network - on – Chip

UNIT I INTRODUCTION TO NOC 9

Introduction to NOC – OSI Layer Rules in NOC - Interconnection Networks in Network-On-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support

UNIT II ARCHITECTURE DESIGN 9

Switching Techniques and Packet Format - Asynchronous FIFO Design - GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design

UNIT III ROUTING ALGORITHM 9

Packet Routing-QOS, Congestion Control and Flow Control – Router Design – Network Link Design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing For 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms

UNIT IV TEST AND FAULT TOLERANCE OF NOC 9

Design-Security in Networks-On-Chips-Formal Verification of Communications in Networks-On Chips-Test and Fault Tolerance For Networks-On-Chip Infrastructures-Monitoring Services For Networks-On-Chips

UNIT V THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP 9

Three-Dimensional Networks-On-Chips Architectures – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation For QOS On-Chip Communication – Networks-On-Chip Protocols-On-Chip Processor Traffic Modeling For Networks-On-Chip

TOTAL:45 PERIODS

OUTCOMES:

At the end of this course, the students will be able to:

1. Compare different architecture design
2. Discuss different routing algorithms
3. Explain three dimensional Networks on Chip architectures
4. Test and design fault tolerant NOC
5. Design three dimensional architectures of NOC

References

1. ChrysostoMOSnicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-On - Chip " Architectures Holistic Design Exploration", Springer.
2. Fayezgebali, Haythamelmiligi, Hqhahedwatheq E1-Kharashi "Networks-On-Chips Theory and Practice CRC Press

3. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-On-Chip Architectures" 2013

4. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-On-Chip" 2014

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	0	2	3	3	0
CO2	3	0	2	3	3	0
CO3	3	0	2	3	3	0
AVG	(9/3)=3	0	(6/3)=2	(9/3)=3	(9/3)=3	0

VL4075 **NANOTECHNOLOGY** **L T P C**
3 0 0 3

OBJECTIVES:

1. Provides knowledge of various industrial applications of Nanotechnology
2. Introduces the theory and practice on Nanomaterials
3. Imparting the state of art of nanotechnology to the society and to the environmental implication
4. To exercise the students' knowledge and imagination of Nanoscience and nanotechnology toward engineering applications coupled with detailed justifications.

UNIT I **NANOTECHNOLOGY** **9**

Background, what is Nanotechnology, types of Nanotechnology and Nano-machines, top down and bottom up techniques, atomic manipulation-Nanodots, semi-conductor quantum dots, self-assembly monolayers, simple details of characterization tools- SEM, TEM, STM, AFM.

UNIT II NANOMATERIALS 9

What are Nanomaterials? Preparation of Nanomaterials- solid state reaction method, Chemical Vapor Deposition, SOL-GELS techniques, electrodeposition, ball milling, introduction to lithography, Pulse Laser Deposition (PLD), applications of Nanomaterials

UNIT III CARBON TUBES 9

New forms of carbon, carbon tubes-types of Nanotubes, formation of Nanotubes, assemblies, purification of carbon Nanotubes, properties of Nanotubes, applications of Nanotubes

UNIT IV OPTICS, PHOTONICS AND SOLAR ENERGY 9

Light and Nanotechnology, interaction of light and Nanotechnology, Nanoholes and photons, solar cells, optically useful Nanostructured polymers, photonic crystals.

UNIT V FUTURE APPLICATIONS 9

MEMS, Nanomachines, Nanodevices, Quantum Computers, Opto-electronic Devices, Quantum Electronic devices, environmental and biological applications.

TOTAL:45 PERIODS

OUTCOMES:

At the end of this course, the students should will be able to:

CO1: understand the bases for introduction to Nanotechnology
CO2: understand the synthesis of Nanomaterials and their application and the impact of Nanomaterials on environment
CO3: acquire knowledge about various kind of Nano materials
CO4: understand the Nanotechnology devices used and their structures
CO5: understand and improve the application of Nanotechnology

REFERENCES

1. Mick Wilson, Kamali Kannangra Geoff Smith, Michelle Simons and Burkhard Raguse,"Nanotechnology-Basic Science and Emerging Technologies", Overseas Press, 2002
2. Mark Ratner and Daniel Ratner, "Nanotechnology-a Gentle Introduction to The Next Big Idea",Prentice Hall,2003
3. Rebecca L Johnson,"Nanotechnology", Lerner Publications,2003
4. Charles P. Poole Jr., "Introduction to Nanotechnogy",Chapman and Hall/CRS,2003

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	0	3	3	0	0
CO2	3	0	3	3	0	0
CO3	3	0	3	3	0	0

CO4	3	0	3	3	0	0
CO5	3	0	3	3	0	0
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(0/0)=0	(0/0)=0

VL4252 **LOW POWER VLSI DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

1: identify sources of power in an IC.
2:identify the power reduction techniques based on technology independent and technology dependent methods
3: identify suitable techniques to reduce the power dissipation
4: estimate power dissipation of various MOS logic circuits
5: develop algorithms for low power dissipation

UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of Limits of Power – Sources of Power Consumption – Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.

UNIT II POWER OPTIMIZATION 9

Logic Level Power Optimization – Circuit Level Low Power Design – Gate Level Low Power Design –Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques – Special Techniques, Adiabatic Techniques – Physical Design, Floor Planning, Placement and Routing.

UNIT IV POWER ESTIMATION 9

Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER CMOS CIRCUITS 9

Synthesis for Low Power – Behavioral Level Transform –Algorithms for Low Power – Software Design for Low Power.

TOTAL:45 PERIODS

OUTCOMES:

At the end of this course, the students should will be able to:
CO1: able to find the power dissipation of MOS circuits
CO2: design and analyze various MOS logic circuits
CO3 :apply low power techniques for low power dissipation
CO4: able to estimate the power dissipation of ICs
CO5: able to develop algorithms to reduce power dissipation by software.

REFERENCES

1. Kaushik Roy and S.C.Prasad, “Low Power CMOS VLSI Circuit Design”, Wiley, 2000
2. J.B.Kulo and J.H Lou, “Low Voltage CMOS VLSI Circuits”, Wiley 1999.
3. James B.Kulo, Shih-Chia Lin, “Low Voltage SOI CMOS VLSI Devices and Circuits”, John Wiley and Sons, Inc. 2001
4. J.Rabaey, “Low Power Design Essentials (Integrated Circuits and Systems)”, Springer, 2009

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	0	2	1	1	0
CO2	2	0	2	2	1	0
CO3	3	0	2	2	1	0
CO4	3	0	2	1	2	0
CO5	2	0	2	2	3	0
AVG	(12/5)=2.4	(0/0)=0	(10/5)=2	(8/4)=2	(8/5)=1.6	(0/0)=0

VE4004 MULTICORE ARCHITECTURE PROGRAMMING **L T P C 3 0 0 3**

OBJECTIVES:

1. Understand the challenges in parallel and multi-threaded programming.
2. Learn about the various parallel programming paradigms, and solutions.

UNIT I MULTI-CORE PROCESSORS **9**

Single Core To Multi-Core Architectures – SIMD And MIMD Systems – Interconnection Networks - Symmetric And Distributed Shared Memory Architectures – Cache Coherence - Performance Issues –Parallel Program Design

UNIT II PARALLEL PROGRAM CHALLENGES **9**

Performance – Scalability – Synchronization And Data Sharing – Data Races – Synchronization Primitives (Mutexes, Locks, Semaphores, Barriers) – Deadlocks And Livelocks – Communication Between Threads (Condition Variables, Signals, Message Queues And Pipes).

UNIT III SHARED MEMORY PROGRAMMING WITH OPENMP **9**

Openmp Execution Model – Memory Model – Openmp Directives – Work-Sharing Constructs – Library Functions – Handling Data And Functional Parallelism – Handling Loops - Performance Considerations

UNIT IV DISTRIBUTED MEMORY PROGRAMMING WITH MPI 9

MPI Program Execution – MPI Constructs – Libraries – MPI Send and Receive – Point-To Point and Collective Communication – MPI Derived Datatypes – Performance Evaluation

UNIT V PARALLEL PROGRAM DEVELOPMENT 9

Case Studies - N-Body Solvers – Tree Search – Openmp and MPI Implementations and Comparison

TOTAL PERIODS:45

OUTCOMES:

At the end of the course, the student should be able to:

1. Illustrate the challenges in parallel and multi threaded programming
2. Explain the various parallel programming paradigms and solutions.
3. Develop shared memory programs using openmp
4. Develop distributed memory programs using mpi
5. Compare and contrast programming for serial processors and parallel processors.

REFERENCES

1. Peter S. Pacheco, “An Introduction To Parallel Programming”, Morgan-Kauffman/Elsevier, 2011.
2. Darryl Gove, “Multicore Application Programming for Windows, Linux, And Oracle Solaris”, Pearson, 2011
3. Michael J Quinn, “Parallel Programming In C With MPI And Openmp”, Tata McGraw Hill

	1	2	3	4	5	6
CO1	3	0	3	3	0	0
CO2	3	0	3	3	0	0
CO3	3	0	3	3	2	0
CO4	3	0	3	3	2	0
CO5	3	0	3	3	0	0
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(4/2)=2	(0/0)=0

VE4005 RECONFIGURABLE COMPUTING L T P C 3 0 0 3

OBJECTIVES:

1. To understand the need for reconfigurable computing
2. To expose the students to various device architectures
3. To examine the various reconfigurable computing systems
4. To expose the students to HDL programming and familiarize with the development environment
5. To develop applications with FPGAs

UNIT I DEVICE ARCHITECTURE 9

General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices – Complex Programmable Logic Devices – FPGAs– Device Architecture - Case Studies.

UNIT II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS 9

Reconfigurable Processing Fabric Architectures – RPF Integration Into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management.

UNIT III PROGRAMMING RECONFIGURABLE SYSTEMS 9

Compute Models - Programming FPGA Applications In HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing.

UNIT IV MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS 9

the Design Flow - Technology Mapping – FPGA Placement And Routing – Configuration Bit stream Generation – Case Studies with Appropriate Tools.

UNIT V APPLICATION DEVELOPMENT WITH FPGAS 9

Case Studies of FPGA Applications – System On a Programmable Chip (SOPC) Designs

TOTAL:45 PERIODS

OUTCOMES:

Upon completion of the course, the students will be able to

1. Identify the need for reconfigurable architectures
2. Discuss the architecture of FPGAs
3. Point out the salient features of different reconfigurable architectures
4. Build basic modules using any HDL
5. Develop applications using any HDL and appropriate tools
6. Design and build an SOPC for a particular application

REFERENCES

1. Maya B. Gokhale and Paul S. Graham, “Reconfigurable Computing: Accelerating Computation With Field-Programmable Gate Arrays”, Springer, 2005.
2. Scott Hauck and Andre Dehon (Eds.), “Reconfigurable Computing – the Theory and Practice of FPGA-Based Computation”, Elsevier / Morgan Kaufmann, 2008.
3. Christophe Bobda, “Introduction To Reconfigurable Computing – Architectures, Algorithms and Applications”, Springer, 2010.

	1	2	3	4	5	6
CO1	3	0	3	3	0	0

CO2	3	0	3	3	0	0
CO3	3	0	3	3	0	0
CO4	3	0	3	3	3	0
CO5	3	0	3	3	3	0
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(6/2)=3	(0/0)=0

VE4071 **HARDWARE SOFTWARE CO-DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

1. To acquire the knowledge about system specification and modelling
2. To learn the formulation of partitioning
3. To study the different technical aspects about prototyping and emulation

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification And Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures With One ASIC, Single-Processor Architectures With Many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping And Emulation Techniques, Prototyping and Emulation Environments, Future Developments In Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-Simulation

TOTAL: 45 PERIODS

OUTCOMES:

At the end of this course, the students should will be able to:

CO1: describe the broad range of system architectures and design methodologies that currently exist and define their fundamental attributes.

Co2: discuss the dataflow models as a state-of-the-art methodology to solve co-design problems and to optimize the balance between software and hardware.

Co3: understand in translating between software and hardware descriptions through co-design methodologies.

Co4: understand the state-of-the-art practices in developing co-design solutions to problems using modern hardware/software tools for building prototypes.

Co5: understand the concurrent specification from an algorithm, analyze its behavior and partition the specification into software (C code) and hardware (HDL) components

TOTAL PERIODS:45

REFERENCES

1. Patrick Schaumont, “a Practical Introduction To Hardware/Software Codesign”, Springer,2010.
2. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Publisher, 1998.
3. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles And Practice”, Kluwer Academic Publisher,1997.
4. Giovanni De Micheli, Rolf Ernst Morgon, “Reading In Hardware/Software Co-Design”, Kaufmann Publisher,2001.

	1	2	3	4	5	6
CO1	3	0	3	3	0	0
CO2	3	0	3	3	0	0
CO3	3	0	3	3	0	0
CO4	3	0	3	3	0	0
CO5	3	0	3	3	0	0
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(0/0)=0	(0/0)=0

II4072 **SYSTEM ON CHIP** **L T P C**

3 0 0 3

OBJECTIVE:

- To introduce architecture and design concepts underlying system on chips.
- Students can gain knowledge of designing SoCs.
- To impart knowledge about the hardware-software design of a modest complexity chip allthe way from specifications, modeling, synthesis and physical design.

UNIT I SYSTEM ARCHITECTURE: OVERVIEW 9

Components of the system – Processor architectures – Memory and addressing – system levelinterconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.

UNIT II PROCESSOR SELECTION FOR SOC 9

Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling – Minimizing pipeline delays – reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.

UNIT III MEMORY DESIGN 9

SoC external memory, SoC internal memory, Scratch pads and cache memory – cache organization and write policies – strategies for line replacement at miss time – split I- and Dcaches – multilevel caches – SoC memory systems – board based memory systems – simple processor/memory interaction.

UNIT IV INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION 9

Bus architectures – SoC standard buses – AMBA, CoreConnect – Processor customization approaches – Reconfigurable technologies – mapping designs onto reconfigurable devices - FPGA based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.

UNIT V FPGA BASED EMBEDDED PROCESSOR 9

Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors andHard Processors – Tool flow for Hardware/Software Co-design –Interfacing Processor with memory and peripherals – Types of On-chip interfaces – Wishbone interface, Avalon Switch Matrix, OPB Bus Interface, Creating a Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning.

TOTAL:45 PERIODS

OUTCOMES:

Upon successful completion of the program the students shall

- Explain all important components of a System-on-Chip and an embedded system, i.e.
- digital hardware and embedded software;
- Outline the major design flows for digital hardware and embedded software;
- Discuss the major architectures and trade-offs concerning performance, cost and power
- consumption of single chip and embedded systems;

REFERENCES:

1. Wayne Wolf, “Modern VLSI Design – System – on – Chip Design”, Prentice Hall, 3rd Edition, 2008.
Wayne Wolf , “Modern VLSI Design – IP based Design”, Prentice Hall, 4th Edition, 2008

VL4073	MEMS AND NEMS	L T P C 3 0 0 3

OBJECTIVES:

1. to introduce the concepts of Micro Electro Mechanical devices.
2. to know the fabrication process of microsystems.
3. to know the design concepts of micro sensors and micro actuators.
4. to familiarize concepts of Quantum Mechanics and Nano systems.

UNIT I OVERVIEW 9

New trends in Engineering and Science: Micro and Nanoscale systems, introduction to design of MEMS and NEMS, MEMS and NEMS – applications, devices and structures. Materials for MEMS: Silicon, Silicon compounds, polymers, metals

UNIT II MEMS FABRICATION TECHNOLOGIES 9

Microsystem Fabrication Processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin Film Depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching Techniques: Dry and Wet Etching, Electrochemical Etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-Like) Technology; Packaging: Microsystems Packaging, Essential Packaging Technologies, Selection of Packaging Materials

UNIT III MICRO SENSORS 9

MEMS Sensors: Design of Acoustic Wave Sensors, Resonant Sensor, Vibratory Gyroscope, Capacitive and Piezo Resistive Pressure Sensors- Engineering Mechanics Behind These Microsensors. Case Study: Piezo-Resistive Pressure Sensor.

UNIT IV MICRO ACTUATORS 9

Design of Actuators: Actuation Using Thermal Forces, Actuation Using Shape Memory Alloys, Actuation Using Piezoelectric Crystals, Actuation using Electrostatic Forces (Parallel Plate, Torsion Bar, Comb Drive Actuators), Micromechanical Motors and Pumps. Case Study: Comb Drive Actuators.

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS 9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave Function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their Quantization, Molecular Wires and Molecular Circuits

TOTAL:45 PERIODS

OUTCOMES:

At the end of this course, the student should be able to:

1. Discuss micro sensors
2. Explain micro actuators
3. Outline nanosystems and Quantum mechanics
4. Design micro actuators for different applications
5. Analyze atomic sturctures

REFERENCES

1. Chang Liu, “Foundations of MEMS”, Pearson Education India Limited, 2006.

2. Marc Madou, “Fundamentals of Microfabrication”, CRC Press 1997.

3. Stephen D. Senturia,” Micro System Design”, Kluwer Academic Publishers,2001

4. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures” CRC Press, 2002.

5. Tai Ran Hsu ,”MEMS and Microsystems Design and Manufacture” ,Tata Mcraw Hill, 2002.

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	0	2	3	0	0
CO2	3	0	2	3	0	0
CO3	3	0	2	3	0	0
AVG	(9/3)=3	0	(6/3)=2	(9/3)=3	0	0

AP4071 **AUTOMOTIVE ELECTRONICS** **L T P C**
3 0 0 3

OBJECTIVES:

- To explain the principle of electronic management system and different sensors used in the systems.
- To know the concepts and develop basic skills necessary to diagnose automotive electronic problems.
- To know Starting, and charging, lighting systems, advanced automotive electrical systems.
- To include electronic accessories and basic computer control.
- To explore practically about the components present in an Automotive electrical and electronics system.

UNIT I FUNDAMENTALS 9

Components for electronic engine management system, open and closed loop control strategies, PID control, Look up tables, introduction to modern control strategies like Fuzzy logic and adaptive control. Switches, active resistors, Transistors, Current mirrors/amplifiers, Voltage and current references, Comparator, Multiplier. Amplifier, filters, A/D and D/A converters.

UNIT II Modern Sensors 9

Film sensors, micro-scale sensors, Particle measuring systems, Vibration Sensors, SMART sensors, Machine Vision, Multi-sensor systems Applications of Sensors: Applications and case studies of Sensors in Automobile Engineering, Aeronautics, Machine tools and Manufacturing processes.

UNIT III **Charging System** **9**

Generation of Direct Current- Shunt Generator Characteristics- Armature Reaction- Third Brush Regulation- Cutout. Voltage and Current Regulators- Compensated Voltage Regulator Alternators Principle and Constructional Aspects and Bridge Rectifiers- New Developments.

UNIT IV **Automotive Transmission Control Systems** **9**

Transmission control - Cruise control – Braking control – Traction control –Suspension control – Steering control – Stability control – Integrated engine control.

UNIT V **Electronics Systems** **9**

Current Trends in Automotive Electronic Engine Management System- Types of EMS Electromagnetic interference Suppression- Electromagnetic Compatibility- Electronic Dashboard Instruments- Onboard Diagnostic System- Security - Warning System infotainment and Telematics.

SUGGESTED ACTIVITIES:

1: Testing of battery, starting systems, charging systems, ignition systems and body controller systems
2: Study of various sensors and actuators used in two wheelers and four wheelers for electronic control.
3: Study of Development of Embedded Systems projects.

OUTCOMES:
At the end of this course the students will be able to:
CO1: Explain the fundamentals, operation, function of various sensors and actuators in engine management systems.
CO2: Explain the Automotive Transmission Control Systems.
CO3: Enumerate the principles, application, construction and specification of different sensors and actuators usable in typical automobile by suitable testing.
CO4: List out the principles and characteristics of charging system components and demonstrate their working with suitable tools.
CO5: Describe the principles and architecture of electronics systems and its components present in an automobile related to instrumentation, control, security and warning systems.

TOTAL PERIODS: 45

REFERENCES

1. Allan Bonnick, “Automotive Computer Controlled Systems”, Butterworth-Heinemann, Elsevier, Indian Edition, 2011.

2. Eric Chowanietz, “Automobile Electronics” by SAE Publications, 1995

3. Tom Weather Jr and Cland C. Hunter, “Automotive Computers and Control System”

Prentice Hall Inc.,1984 New Jersey.

4. R.K. Jurgen, "Automotive Electronics Handbook", McGraw Hill 2 nd Edition,1995.

5. William B Ribbens, "understanding automotive electronics", 5th edition - Butter worth Heinemann Woburn, 1998.

VE4006 EMBEDDED WIRELESS SENSOR NETWORKS **L T P C 3 0 0 3**

OBJECTIVES:

1. To discuss the overview of wireless sensor networks
2. To familiarize the architecture of different networks
3. To get knowledge about various physical layer and MAC protocols
4. To acquire knowledge about different types of smart sensors used for designing the embedded system
5. To know about the implementation of protocols on WSN in various applications

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS **9**

Challenges for Wireless Sensor Networks - Characteristics Requirements - Required Mechanisms, Difference Between Mobile Ad-Hoc and Sensor Networks- Enabling Technologies for Wireless Sensor Networks. Single-Node Architecture - Hardware Components - Energy Consumption Sensor Nodes Operating Systems and Execution Environments - Sensor Node Examples: Eyes, Mica, Micaz Motes.

UNIT II NETWORK ARCHITECTURE **9**

Sensor Network Scenarios – Optimization Goals and Figure of Merit – Design Principles for WSNs – Gateway Concepts.

UNIT III PHYSICAL LAYER AND MAC PROTOCOLS **9**

Wireless Channel and Communication Fundamentals – Physical Layer and Transceiver Design Considerations In WSN – Fundamentals of MAC Protocols low Duty Cycle Protocols and Wakeup Concepts – Contention Based Protocols - Schedule Based Protocols – IEEE 802.15.4 MAC Protocol.

UNIT IV SMART SENSORS **9**

Introduction To Smart Sensors – Signal Conditioning Circuits – Architecture of Smart Sensors Humidity Sensors – Soil Moisture Sensors– Temperature Sensors – Color Sensors – Level sensors.

UNIT V APPLICATIONS AND PROTOCOL IMPLEMENTATION ON WSN **9**

Home Control - Medical Applications - Civil And Environmental Engineering Applications – Wildfire Monitoring - Habitat Monitoring. Embedding Leach Protocol On ARM 7 TDM Microcontroller Using Embedded C Language - Embedding Cryptographic Algorithms On ARM 7 TDM Microcontroller Using Embedded C Language – FPGA Based Customizable Event Driven Architecture

TOTAL:45 PERIODS

OUTCOMES:

At the end of this course, the students should will be able to:

1. Explain the basics of wireless sensor networks.
2. Discuss about the sensor network components, architecture and design principles of WSN
3. Explain the need of physical layer design challenges and MAC protocols.
4. Design the smart sensors and applications of WSN.
5. Improved employability and entrepreneurship capacity due to knowledge upgradation on recent trends in embedded systems design.

REFERENCES

1. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazemsohraby, Daniel Minoli, & Taiebznati, "Wireless Sensor Networks technology, Protocols and Applications", John Wiley, 2012.
3. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.
4. Bhaskar Krishnamachari, "Networking Wireless Sensors", Cambridge Press, 2005.
5. Mohammad Ilyas and Imad Mahgaob, "Handbook of Sensor Networks: Compact Wireless and Wired Sensing Systems", CRC Press, 2005.
6. **Hdger Karl Andreas Willig,"Protocols and Architectures for Wireless Sensor Networks", Wiley 2007**

	1	2	3	4	5	6
CO1	3	0	3	3	0	0
CO2	3	0	3	3	0	0
CO3	3	0	3	3	0	0
CO4	3	0	3	3	0	2
CO5	3	0	3	3	0	2
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(0/0)=0	(4/2)=2

VE4007 NETWORK EMBEDDED APPLICATIONS **L T P C 3 0 0 3**

OBJECTIVES:

1. To give an introduction to and developing deeply embedded systems
2. To familiarize the architecture and protocols in WSN
3. To briefly study the application areas of network embedded systems

UNIT I NETWORK EMBEDDED SYSTEMS: AN INTRODUCTION 9

Networked Embedded Systems: An Overview - Middleware Design and Implementation for Networked Embedded Systems

UNIT II WIRELESS SENSOR NETWORKS 9

Introduction To WSNS- Architecture for WSNS- Localization & Synchronization for WSN- Time Sync Issues & Resource Aware Localization

UNIT III POWER AND ENERGY IN WSN 9

Networking In WSN Power Aware Routing Issues & Protocols- MAC for WSN Energy Efficient MAC Protocols- Distributed Signal Processing In Sensor Networks- Sensor Network Security

UNIT IV AUTOMOTIVE NETWORKED EMBEDDED SYSTEMS 9

Time – Triggered Communication- Networks In Automotive Systems - Controller Area Networks, Flex Ray Communications, Lin Self-Study Automotive Examples Volcano

UNIT V INDUSTRIAL AUTOMATION 9

Introduction To Industrial Automation-Field Bus, Real-Time Ethernet-Home Automation Home Automation

TOTAL :45 PERIODS

OUTCOMES:

At the end of this course, the students should will be able to:

CO1: understand the basics of network systems

2. discuss about the sensor network components, architecture and design principles of WSN

3. Explain the need MAC protocols and energy conservation

4. application of networked automotive system

5. design and development of home automation

REFERENCES

1. R.Zurawski, Network Embedded Systems, Crc Press, 2009.
2. G.Pottie, W.Kaiser, Principles of Embedded Networked System Design
3. Raj Kamal, Embedded Systems, Tata McGraw Hill, New Delhi, 2003
4. **Francine Krief,"Communicating Embedded System" Wiley 2010.**

	1	2	3	4	5	6
CO1	3	0	3	3	0	0
CO2	3	0	3	3	0	0
CO3	3	0	3	3	0	0
CO4	3	0	3	3	0	2
CO5	3	0	3	3	1	2
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(1/1)=1	(4/2)=2

VL4253 RFIC DESIGN L T P C
3 0 0 3

OBJECTIVES:

- to study the various impedance matching techniques used in RF circuit design.
- to understand the functional design aspects of LNAs, Mixers, PLLs and VCOs.
- to understand frequency synthesis.

UNIT I IMPEDANCE MATCHING IN AMPLIFIERS 9

Definition of 'Q', Series Parallel Transformations of Lossy Circuits, Impedance Matching Using 'L', 'Pi' and T Networks, Integrated Inductors, Resistors, Capacitors, Tunable Inductors, Transformers

UNIT II AMPLIFIER DESIGN 9

Noise Characteristics of MOS Devices, Design of CG LNA and Inductor Degenerated LNAs. Principles of RF Power Amplifiers Design

UNIT III ACTIVE AND PASSIVE MIXERS 9

Qualitative Description of the Gilbert Mixer - Conversion Gain, and Distortion and Noise , Analysis of Gilbert Mixer – Switching Mixer - Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - a Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV OSCILLATORS 9

LC Oscillators, Voltage Controlled Oscillators, Ring Oscillators, Delay Cells, Tuning Range in Ring Oscillators, Tuning in LC Oscillators, Tuning Sensitivity, Phase Noise in Oscillators, Sources of Phase Noise

UNIT V PLL AND FREQUENCY SYNTHESIZERS 9

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase Noise in PLL, Loop Bandwidth, Basic Integer-N Frequency Synthesizer, Basic Fractional-N Frequency Synthesizer

TOTAL:45 PERIODS

OUTCOMES:

At the end of this course, the students should will be able to:

CO1: to understand the principles of operation of an RF receiver front end
CO2: to design and apply constraints for LNAs, Mixers and frequency synthesizers
CO3: to analyze and design mixers
CO4: to design different types of oscillators and perform noise analysis
CO5: to design PLL and frequency synthesizer

REFERENCES

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" Mcgraw-Hill, 1999
4. Jia-Sheng Hong, "Microstrip Filters for RF/Microwave Applications", Wiley, 2001
5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	0	3	3	1	0
CO2	3	0	3	3	2	0
AVG	(6/2)=3	0	(6/2)=3	(6/2)=3	(3/2)=1.5	0

AP4077 SENSORS AND ACTUATORS L T P C
3 0 0 3

OBJECTIVES:

- Understand static and dynamic characteristics of measurement systems.
- Study various types of sensors.
- Study different types of actuators and their usage.
- Study State-of-the-art digital and semiconductor sensors.

UNIT I INTRODUCTION TO MEASUREMENT SYSTEMS 9

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance characteristics: static and dynamic characteristics of measurement systems, zero-order, first-order, and second-order measurement systems and response.

UNIT II RESISTIVE AND REACTIVE SENSORS 9

Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & application to LVDT.

UNIT III SELF-GENERATING SENSORS 9

Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper and low-drift amplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers.

UNIT IV ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS 9

Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.

UNIT V DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS 9

Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, MOSFET transistors, CCD imaging sensors , ultrasonic sensors, fiber-optic sensors.

TOTAL: 45 PERIODS

OUTCOMES:

Upon completion of the course the student will be able to :

- Compare Actuators
- Evaluate digital sensors and semiconductor device sensors
- Discuss Self-generating sensors

REFERENCES BOOKS:

1. Andrzej M. Pawlak Sensors and Actuators in Mechatronics Design and Applications, 2006.
2. D. Johnson, “Process Control Instrumentation Technology”, 8th Ed, 2014, John Wiley and Sons.
3. D.Patranabis, “Sensors and Transducers”, TMH 2003.
4. E.O. Doeblin, “Measurement System: Applications and Design”, McGraw Hill publications,1996
5. Graham Brooker, Introduction to Sensors for ranging and imaging, Yesdee, 2009.
6. Herman K.P. Neubrat, “Instrument Transducers – An Introduction to Their Performance and Design”, Oxford University Press. 22,1999.
7. Ian Sinclair, Sensors and Transducers, Elsevier, 3rd Edition, 2011.
8. Jon Wilson , “Sensor Technology Handbook”, Newne 2004.
9. Kevin James, PC Interfacing and Data acquisition, Elsevier, 2011.
10. Ramon PallásAreny, John G. Webster, “Sensors and Signal conditioning”, 2nd edition, John Wiley and Sons, 2000.

11. Sensors and Actuators: Control System Instrumentation, Clarence W. de Silva CRC Press, 2007

VE4008 REAL TIME OPERATING SYSTEMS

L	T	P	C
3	0	2	4

OBJECTIVES:

1. To learn about significance and usage of Real Time Operating System
2. To learn about different scheduling strategies and optimization principles
3. To learn about the resource allocation or sharing process involved in RTOS
4. To study about the different firmware and tools related to RTOS development
5. To design and develop an innovative real time embedded system

UNIT – I REAL TIME EMBEDDED SYSTEMS 9

Introduction - History of Real Time Systems And Embedded Systems - Real Time Services and Standards - System Resources - Analysis - Service Utility - Scheduling Classes - Cyclic Executive - Scheduler Concepts- Real Time Operating System - Thread Safe Reentrant Functions

UNIT – II RESOURCES AND SERVICES 9

Processing - Resources - Memory –Multiresource Services : Blocking, Deadlock, Livelock, Critical Sections To Protect Shared Resources, Priority Inversion, Power Management And Processor Clock Modulation - Soft Real Time Services : Missed Deadlines, Quality of Service, Alternatives To Rate Monotonic Policy, Mixed Hard and Soft Real Time Services

UNIT – III REAL TIME EMBEDDED COMPONENTS 9

Hardware Components - Firmware Components - RTOS System Software - Software Application Components - Traditional Hard Real Time Operating Systems : Asymmetric Multicore Processing And Symmetric Multi-Core Processing - Processor Core Affinity - SMP Support Models - RTOS Hypervisors - Open Source Real Time Operating Systems

UNIT – IV INTEGRATING EMBEDDED LINUX 9

Integrating Embedded Linux Into Real Time Systems - Debugging Components - Performance Tuning - High Availability And Reliability Design - Hierarchical Approaches for Fail-Safe Design.

UNIT – V CASE STUDIES 9

System Life Cycle - Continuous Media Applications - Video and Audio Processing - Robotic Applications - Computer Vision Applications

TOTAL: 45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

Laboratory Exercises On Task Scheduling

1. Create An Application That Creates Two Tasks That Wait On a Timer Whilst the Main Task Loops.
2. Write Simple Applications Using Linux
3. Design of Plant Control System

OUTCOMES:

On successful completion of this course, students will be able to

CO1: complete understanding of scheduling algorithm and process
CO2: better understanding on firmware and tools related to the development of RTOS
CO3: to be able to design and develop an embedded system with RTOS functionality
CO4: to be able to design and develop the systems in Linux environments
CO5: to be able to develop large real-time embedded systems

REFERENCES:

1. Sam Siewert, John Pratt, "Real-Time Embedded Components and Systems With Linux And Rtos", Mercury Learning And Information Llc, 2016.
2. Jonathan W. Valvano, "Embedded Systems: Real Time Operating Systems for ARM Cortex-M Microcontrollers", Createspace Independent Publishing Platform, Fourth Edition, 2017.
3. Giorgio C. Buttazzo, "Hard Real-Time Computing Systems - Predictable Scheduling Algorithms And Applications", Springer Science+Buisness Media, LLC, Third Edition, 2011.
4. Albert M. K. Cheng, "Real-Time Systems - Scheduling, Analysis And Verification", a John Wiley & Sons Inc Publication, 2002.
5. Wang K.C., “Embedded And Real Time Operating System”, Springer, 2017

	PO					
	1	**2**	**3**	**4**	**5**	**6**

CO1	3	0	3	3	0	0
CO2	3	0	3	3	0	0
CO3	3	0	3	3	0	0
CO4	3	0	3	3	0	0
CO5	3	0	3	3	0	0
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(0/0)=0	(0/0)=0

VE4009 **EMBEDDED NETWORKING** **L T P C**
3 0 2 4

OBJECTIVES:

1. To learn the concepts of serial and parallel communication protocols
2. To understand the application development using USB and CAN bus for PIC microcontrollers
3. To learn the basics of ethernet
4. To learn the application development using embedded internet
5. To learn the wireless sensor network communication protocols

UNIT – I COMMUNICATION PROTOCOLS 9

Serial/Parallel Communication – Serial Communication Protocols -RS 232 Standard – RS 485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel Port Programming - PCI Bus Protocol.

UNIT – II USB AND CAN BUS 9

USB Bus – Introduction – Speed Identification On the Bus – USB States – USB Bus Communication: Packets –Data Flow Types –Enumeration –Descriptors –PIC Microcontroller USB Interface – CAN Bus – Introduction - Basic Concepts & Definitions-Identifiers & Arbitration-Robustness & Flexibility-Message Formats-Error Handling -PIC Microcontroller CAN Interface –a Simple Application With CAN.

UNIT – III ETHERNET BASICS 9

Elements of a Network – Inside Ethernet – Building a Network: Hardware Options – Cables, Connections and Network Speed – Design Choices: Selecting Components –Ethernet Controllers – Using the Internet In Local And Internet Communications – Inside the Internet Protocol.

UNIT – IV EMBEDDED ETHERNET 9

Exchanging Messages Using UDP And TCP – Serving Web Pages With Dynamic Data – Serving Web Pages That Respond To User Input – Email for Embedded Systems – Using FTP.

UNIT – V EMBEDDED WIRELESS SENSOR NETWORKS 9

Wireless Sensor Networks –Introduction To WSN-Challenges for WSNs - Characteristic Requirements - Required Mechanisms - Single-Node Architecture -Hardware Components-Energy Consumption of Sensor Nodes-Operating Systems and Execution Environments-Some Examples of Sensor Nodes.

TOTAL: 45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1. **Write a Simple Application Program USB and PIC Interface.**
2. Write a Simple Application Program Using CAN And PCI.
3. Write a Program for Email Transferring Using UDP And TCP
4. Write a Program for Energy Harvesting In WSN Node
5. Develop An Application Using Embedded Wireless Sensor Networks

OUTCOMES:

On successful completion of this course, students will be able to

1. analyze the wired and wireless network protocols
2. Design an application using embedded networking
3. Analyze the basics of Ethernet
4. incorporate networks in embedded systems
5. Analyze the basics of wireless sensor networks

REFERENCES:

1. Frank Vahid, Tony Givargis, “Embedded Systems Design: a Unified Hardware/Software Introduction” - John & Wiley Publications, 2006
2. Jan Axelson, “Parallel Port Complete: Programming, Interfacing and Using the PCs Parallel Printer Port” - Penram Publications, 1996.
3. Dogan Ibrahim, “Advanced PIC Microcontroller Projects In C: From USB To RTOS With the PIC18f Series” - Elsevier 2008.
4. Jan Axelson, “Embedded Ethernet and Internet Complete”, Penram Publications, 2003.
5. Bhaskar Krishnamachari, Networking, Wireless Sensors - Cambridge Press 2005.
6. Olaf Pfeiffer, Andrew Ayre and Christian Keydel, “Embedded Networking With CAN And CAN Open”, Second Edition Published By Copperhill Media Corporation, 2003.
7. Holgerkarl, Andreas Willig, “Protocols and Architectures for Wireless Sensor Networks”, John Wiley,2005

	1	2	3	4	5	6
CO1	3	0	3	2	0	0
CO2	3	0	3	2	0	0
CO3	3	0	3	2	0	0
CO4	3	0	3	2	0	0
CO5	3	0	3	2	0	0

AVG	(15/5)=3	(0/0)=0	(15/5)=3	(10/5)=2	(0/0)=0	(0/0)=0

IF4072 **COMPUTER VISION** **L T P C**
3 0 0 3

OBJECTIVES:

1: Articulate & apply standard computer vision concepts
2: Implement standard image processing tasks
3: Applying Clustering concept for Image Classification
4: Identify practical constraints in computer vision application
5: Architecture of an existing computer vision pipeline based on deep learning models

UNIT I COMPUTER VISION **8**

About Computer Vision. Components of an Image Processing System. Image Resolution. Image Formats. Colour Spaces. Fundamental of Image Processing. Visual Inspection System. Biomedical Imaging Methods. Image Thresholding. Based Image Retrieval. Human Visual Inception. Image Formation. Geometric Properties. 3D Imaging. Stereo Images.

UNIT II PIXEL-BASED MANIPULATIONS & TRANSFORMATION **8**

Visual properties. Pixel colour manipulation. Colour Change with Pixel Position. Colour Change with Pixel Distance. Colour Change with Trigonometric Functions. Randomness. Drawing with existing images. Blending multiple images. Image transformation. Image orientation. Image resizing. Affine transform. Known Affine Transformations. Unknown Affine Transformations. Perspective transform. Linear vs. polar coordinates. Three-dimensional space. General pixel mapping.

UNIT III STRUCTURE IDENTIFICATION **11**

Image preparation. Conversion to grayscale. Conversion to a black-and-white image. Morphological operations (erode, dilate). Blur operations (smoothing)Edge detection. First Derivative Edge Detectors. Second Derivative Edge Detectors. Multispectral Edge Detection. Line detection. Circle detection. Contours processing. Finding the contours. Bounding box. Minimum area rectangle. Convex hull. Polygon approximation. Testing a point in contour. Checking intersection. Shape detection. Moravec Corner Detection. Harris Corner Detection. FAST Corner Detection. SIFT.

UNIT IV CLUSTERING IMAGES & IMAGE RETRIEVAL **9**

About Transfer Learning. Extract features. SciPy Clustering Package. K-Means Clustering. Clustering Images. Principal Components. Clustering Pixels. Hierarchical Clustering. Spectral Clustering. Fast Fourier Transforms. -Based Image Retrieval. Indexing Images. Searching the Database for Images. Querying with an Image. Benchmarking and Plotting the Results. Ranking Results Using Geometry.

UNIT V IMAGE CLASSIFICATION USING DEEP LEARNING **9**

Working with Image Datasets. k-NN: A Simple Classifier. k-NN Hyperparameters. Gradient Descent. Loss Functions. Stochastic Gradient Descent (SGD). Regularisation. The Perceptron Algorithm. Backpropagation and Multi-layer Networks. Weight Initialization. Constant Initialization. Uniform and Normal Distributions. CNN Building Blocks. Image Classification.

SUGGESTED ACTIVITIES:

1: Identify and List various noises in the Image.
2: Identify Image Manipulation
3: Add colour descriptors and improve the search results.
4: Hierarchical k-means is a clustering method that applies k-means recursively to the clusters to create a tree of incrementally refined clusters
5: Image Classification using CNN

OUTCOMES:

CO1: Understand the basic knowledge, theories and methods of computer vision.
CO2: to understand the essentials of image processing concepts through mathematical interpretation.
CO3: Demonstrate a knowledge of a broad range of fundamental image processing and image analysis techniques
CO4: Apply Clustering algorithms for clustering.
CO5: Analyse cognitive tasks including image classification, recognition and detection through deep learning.

TOTAL:45 PERIODS

REFERENCES

1. Pro Processing for Images and Computer Vision with OpenCV, Bryan WC Chung, Apress, 2017
2. Programming Computer Vision with Python, Jan Erik Solem, O'Reilly Media, 2012
3. A PRACTICAL INTRODUCTION TO COMPUTER VISION WITH OPENCV, Kenneth Dawson-Howe, Wiley, 2014
4. Practical Computer Vision Applications Using Deep Learning with CNNs: With Detailed Examples in Python Using TensorFlow and Kivy, Ahmed Fawzy Gad, Apress. 2018
5. Computer Vision Principles, Algorithms, Applications, Learning E.R. Davies, Academic Press, 5th edition, 2017

VE4072	REAL TIME EMBEDDED SYSTEM DESIGN	L T P C 3 0 2 4

OBJECTIVES:

1. To understand the basics of embedded system and ARM architecture
2. To understand the RTOS concepts like scheduling and memory management related to the embedded system
3. To learn about the programming aspects of RTOS
4. To learn the different protocols of embedded wireless application
1. To understand concepts involved in the design of hardware and software components for an embedded system

UNIT I INTRODUCTION 9

Real Time System – Embedded Systems – Architecture of Embedded System – Simple Programming for Embedded System – Process of Embedded System Development – Pervasive Computing – Information Access Devices – Smart Cards – Microcontrollers – ARM Processor - Real Time Microcontrollers.

UNIT II EMBEDDED/REAL TIME OPERATING SYSTEM 9

Operating System Concepts: Processes, Threads, Interrupts, Events - Real Time Scheduling Algorithms - Memory Management – Overview of Operating Systems for Embedded, Real Time Handheld Devices – Target Image Creation – Programming In Linux, Rtlinux, Vxworks, Microcontroller Operating System Overview.

UNIT III CONNECTIVITY 9

Wireless Connectivity - Bluetooth – Other Short Range Protocols – Wireless Application Environment – Service Discovery – Middleware.

UNIT IV REAL TIME UML 9

Requirements Analysis – Object Identification Strategies – Object Behaviour – Real Time Design Patterns.

UNIT V SOFTWARE DEVELOPMENT AND APPLICATION 9

Concurrency – Exceptions – Tools – Debugging Techniques – Optimization –Interfacing Digital Camera With USB Port.

TOTAL: 45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1. Read Input From Switch And Automatic Control/Flash LED for ARM Processor
2. Laboratory Exercises On Task Scheduling
3. Simple Program In Linux, Rtlinux And Vxworks
4. Develop a Real Time Security Monitoing System

COURSE OUTCOMES:

On successful completion of this course, students will be able to

1. Make a choice of suitable embedded processor for a given application
2. Design the hardware and software for the embedded system
3. Design and develop the real time kernel/operating system functions, task control block structure and analyze different task states
4. Implement different types of inter task communication and synchronization techniques
5. To be able to know about the aspects embedded connectivity in real time systems

REFERENCES:

1. R.J.a.Buhr, D.L.Bailey, “An Introduction To Real-Time Systems”, Prentice-Hall International,1999.
2. David E-Simon, “An Embedded Software Primer”, Pearson Education, 2007.
3. C.M.Krishna, Kang G.Shin, “Real Time Systems”, Mc-Graw Hill, 2010.
4. B.P.Douglass, “Real Time Uml - Advances In the UML for Real-Time Systems, 3rd Edition Addison-Wesley, 2004.
5. K.V.K. Prasad, “Embedded/Real Time Systems: Concepts, Design And Programming”, Dream Tech Press, Black Book, 2005.
6. R.Barnett, L.O.Cull, S.Cox, “Embedded C Programming and the Microchip PIC ”, Thomason Learning, 2004.
7. Wayne Wolf, “Computers As Components - Principles of Embedded Computer System Design”, Mergen Kaufmann Publisher, 2006.
8. Sriram V Iyer, Pankaj Gupta, “Embedded Real Time Systems Programming”, Tata Mc-Graw Hill, 2004.

	1	2	3	4	5	6
CO1	3	0	3	3	2	0
CO2	3	0	3	3	2	0
CO3	3	0	3	3	2	0
CO4	3	0	3	3	2	0
CO5	3	0	3	3	2	0
Avg	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(10/5)=2	(0/0)=0

VE4010 PERVASIVE COMPUTING **L T P C**
3 0 2 4

OBJECTIVES:

1. To understand the characteristics and principles of pervasive computing and the solutions that are in use
2. To realize the role of wireless protocols in shaping the future internet
3. To design and implement pervasive applications
4. To introduce the enabling technologies of pervasive computing

UNIT I PERVASIVE COMPUTING CONCEPTS 9

Perspectives of Pervasive Computing, Challenges, Technology; the Structure and Elements of Pervasive Computing Systems: Infrastructure and Devices, Middleware for Pervasive Computing Systems, Pervasive Computing Environments

UNIT II CONTEXT COLLECTION, USER TRACKING, AND CONTEXT REASONING 9

Resource Management In Pervasive Computing: Efficient Resource Allocation In Pervasive Environments, Transparent Task Migration, Implementation and Illustrations.

UNIT III HCI INTERFACE IN PERVASIVE ENVIORNMENTS 9

HCI Service and Interaction Migration, Context- Driven HCI Service Selection, Scenario Study: Video Calls At a Smart Office, a Web Service– Based HCI Migration Framework .

UNIT IV PERVASIVE MOBILE TRANSACTIONS 9

Mobile Transaction Framework, Context-Aware Pervasive Transaction Model, Dynamic Transaction Management, Formal Transaction Verification, Evaluations

UNIT V CASE STUDIES 9

ICAMPUS Prototype, IPSPACE: AN IPV6-Enabled Intelligent Space

TOTAL:45 PERIODS

PRACTICAL EXERCISES: **30 PERIODS**

1. To Design the Software for Mobile Phones Using Symbion Os

Text String Handling
Graphical Application
Dialog Application
Drawing Application
File Handling Operations

2. Application Level- To Study New HCI Techniques for Small Mobile Devices And Embedded Devices.

3. Case Studies- Projects In Pervasive Computing- To Explore Wearable And Handheld Computing And Their Enabling Technologies

OUTCOMES:

At the end of this course, the students should will be able to:

1. Outline the basic problems, performance requirements of pervasive computing applications, and the trends of pervasive computing and its impacts on future computing applications and society
2. Analyze and compare the performance of different data dissemination techniques and algorithms for mobile real-time applications
3. Analyze the performance of different sensor data management and routing algorithms for sensor networks
4. Develop an attitude to propose solutions with comparisons for problems related to pervasive computing system through investigation
5. Study on application on IPv6.

TOTAL PERIODS:45

REFERENCES

1. Minyi Guo, Jingyu Zhou, Feilong Tang, Yao Shen ,"Pervasive Computing: Concepts, Technologies And Applications", CRC Press, 2016.
2. Obaidat, Mohammad S., Mieso Denko, And Isaac Woungang, Eds. Pervasive Computing And Networking. John Wiley & Sons, 2011.
3. Laurence T. Yang, Handbook On Mobile and Ubiquitous Computing Status and Perspective, 2012, CRC Press
4. Seng Loke, Context-Aware Computing Pervasive Systems, Auerbach Pub., New York, 2007.
5. Uwe Hansmann Etl , Pervasive Computing, Springer, New York,2001.

	PO					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	0	3	3	0	0
CO2	3	0	3	3	3	0
CO3	3	0	3	3	3	0

CO4	3	0	3	3	3	0
CO5	3	0	3	3	3	0
AVG	(15/5)=3	(0/0)=0	(15/5)=3	(15/5)=3	(12/4)=3	(0/0)=0

VE4011 **PHYSICAL DESIGN AUTOMATION** **L T P C**
3 0 2 4

OBJECTIVES:

1. Understand the concepts of physical design process such as partitioning, floorplanning, placement and routing.
2. Discuss the concepts of design optimization algorithms and their application to physical design automation.
3. Understand the concepts of simulation and synthesis in VLSI design automation
4. Formulate CAD design problems using algorithmic methods

UNIT I INTRODUCTION 9

Layout and Design Rules, Materials for VLSI Fabrication, Basic Algorithmic Concepts for Physical Design, Physical Design Processes and Complexities. Partition: Kernigham-Lin's Algorithm, Fiduccia Mattheyes Algorithm, Krishnamurthy Extension, Hmetis Algorithm, Multilevel Partition Techniques.

UNIT II FLOOR-PLANNING: 9

Planning: Hierarchical Design, Wire Length Estimation, Slicing and Non-Slicing Floor Plan, Polar Graph Representation, Operator Concept, Stockmeyer Algorithm for Floor Planning, Mixed Integer Linear Program.

UNIT III PLACEMENT 9

Design Types: ASICS, SOC, Microprocessor RLM; Placement Techniques: Simulated Annealing, Partition Based, Analytical, and Hall's Quadratic; Timing and Congestion Considerations

UNIT IV ROUTING 9

Detailed, Global and Specialized Routing, Channel Ordering, Channel Routing Problems and Constraint Graphs, Routing Algorithms, Yoshimura And Kuh's Method, Zone Scanning and Net Merging, Boundary Terminal Problem, Minimum Density Spanning Forest Problem, Topological Routing, Cluster Graph Representation.

UNIT V SEQUENTIAL LOGIC OPTIMIZATION AND CELL BINDING 9

State Based Optimization, State Minimization, Algorithms; Library Binding and Its Algorithms, Concurrent Binding.

TOTAL:45 PERIODS

PRACTICAL EXERCISES: **30 PERIODS**

1. Graph Algorithms
   - Graph Search Algorithms
   - Spanning Tree Algorithm
   - Shortest Path Algorithm
   - Steiner Tree Algorithm
2. Partitioning Algorithms
   - Group Migration Algorithms
   - Simulated Annealing And Evolution Algorithms
   - Metric Allocation Method
3. Floor Planning Algorithms
   - Constraint Based Methods
   - Integer Programming Based Method
   - Rectangular Dualization Based Methods
   - Hierarchical Tree Based Methods
   - Simulated Evolution Algorithms
   - Time Driven Floor planning Algorithms
4. Routing Algorithms
   - Two Terminal Algorithms
   - Multi Terminal Algorithm

OUTCOMES:

At the end of this course, the students should will be able to:

1. Students can know how to place the blocks and how to partition the blocks while for designing the layout for IC.
2. Students can solve the performance issues in circuit layout.
3. Students are able to analyze physical design problems and employ appropriate automati on algorithms for partitioning, floor planning, placement and routing
4. Students can decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing
5. Students can analyze circuits using both analytical and CAD tools

TOTAL PERIODS:45

REFERENCES

1. Sarrafzadeh, M. and Wong, C.K, “An Introduction to VLSI Physical Design”, 4th Edition, Mc Graw-Hill
2. Wolf. W, “Modern VLSI Design System on Silicon”, 2nd Ed., Pearson Education.
3. Dreschler, “Evolutionary Algorithms for VLSI CAD ”, 3rd Edition, Springer.
4. Sait, S.M, And Youssef, “VLSI Physical Design Automation: Theory And Practice”, 1999, World Scientific Publishing Company.
5. Sherwani, “Algorithms for VLSI Physical Design Automation”, 2nd Edition, Kluwer

	1	2	3	4	5	6
CO1	3	0	3	3	2	0
CO2	3	0	3	3	2	0

CO3	**3**	**0**	**3**	**3**	**2**	**0**
CO4	**3**	**0**	**3**	**3**	**2**	**0**
CO5	**3**	**0**	**3**	**3**	**2**	**0**
Avg	**(15/5)=3**	**(0/0)=0**	**(15/5)=3**	**(15/5)=3**	**(10/5)=2**	**(0/0)=0**

AUDIT COURSES

AX4091 ENGLISH FOR RESEARCH PAPER WRITING **L T P C**
2 0 0 0

COURSE OBJECTIVES

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

UNIT I INTRODUCTION TO RESEARCH PAPER WRITING **6**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II PRESENTATION SKILLS **6**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III TITLE WRITING SKILLS **6**

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV RESULT WRITING SKILLS **6**

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V VERIFICATION SKILLS **6**

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission

TOTAL: 30 PERIODS

COURSE OUTCOMES

CO1 –Understand that how to improve your writing skills and level of readability

CO2 – Learn about what to write in each section
CO3 – Understand the skills needed when writing a Title
CO4 – Understand the skills needed when writing the Conclusion
CO5 – Ensure the good quality of paper at very first-time submission

REFERENCES:

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
3. Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
4. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.

AX 4092 DISASTER MANAGEMENT L T P C
2 0 0 0

COURSE OBJECTIVES

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT I INTRODUCTION 6

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II REPERCUSSIONS OF DISASTERS AND HAZARDS 6

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III DISASTER PRONE AREAS IN INDIA 6

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT IV DISASTER PREPAREDNESS AND MANAGEMENT 6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V RISK ASSESSMENT 6

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival

TOTAL : 30 PERIODS

COURSE OUTCOMES:

CO1: Ability to summarize basics of disaster

CO2: Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.

CO3: Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

CO4: Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

CO5: Ability to develop the strengths and weaknesses of disaster management approaches

REFERENCES:

1. Goel S. L., Disaster Administration And Management Text And Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2. NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company,2007.
3. Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences And Reflections", Prentice Hall OfIndia, New Delhi,2001.

AX4093 CONSTITUTION OF INDIA L T P C
2 0 0 0

COURSE OBJECTIVES:

Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.

UNIT I HISTORY OF MAKING OF THE INDIAN CONSTITUTION

History, Drafting Committee, (Composition & Working)

UNIT II PHILOSOPHY OF THE INDIAN CONSTITUTION

Preamble, Salient Features

UNIT III CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES

Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT IV ORGANS OF GOVERNANCE

Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive,

President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V LOCAL ADMINISTRATION

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy(Different departments), Village level:Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT VI ELECTION COMMISSION

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization
- of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

SUGGESTED READING

1. The Constitution of India,1950(Bare Act),Government Publication.
2. Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,1st Edition, 2015.
3. M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

AX4094 நற்றமிழ் இலக்கியம் L T P C
2 0 0 0

UNIT I சங்க இலக்கியம் 6

1.தமிழின் துவக்க நூல் தொல்காப்பியம்
– எழுத்து, சொல், பொருள்
2.அகநானூறு (82)
- இயற்கை இன்னிசை அரங்கம்
3.குறிஞ்சிப் பாட்டின் மலர் க்காட்சி
4.புறநானூறு (95,195)
- போரை நிறுத்திய ஔவையார்

UNIT II **அறநெறித் தமிழ்** **6**

1. அறநெறி வகுத்த திருவள்ளுவர்
- அறம் வலியுறுத்தல், அன்புடைமை, ஒப்புரவறிதல், ஈகை, புகழ்

2. பிற அறநூல்கள் - இலக்கிய மருந்து
– ஏலாதி, சிறுபஞ்சமூலம், திரிகடுகம், ஆசாரக்கோவை (தூய்மையை வலியுறுத்தும் நூல்)

UNIT III **இரட்டைக் காப்பியங்கள்** **6**

1. கண்ணகியின் புரட்சி
- சிலப்பதிகார வழக்குரை காதை

2. சமூகசேவை இலக்கியம் மணிமேகலை
- சிறைக்கோட்டம் அறக்கோட்டமாகிய காதை

UNIT IV **அருள்நெறித் தமிழ்** **6**

1. சிறுபாணாற்றுப்படை
- பாரி முல்லைக்குத் தேர் கொடுத்தது, பேகன் மயிலுக்குப் போர் வைகொடுத்தது, அதியமான் ஔவைக்கு நெல்லிக்கனி கொடுத்தது, அரசர் பண்புகள்

2. நற்றிணை
- அன்னைக்குரிய புன்னை சிறப்பு

3. திருமந்திரம் (617, 618)
- இயமம் நியமம் விதிகள்

4. தர்மச் சாலையை நிறுவிய வள்ளலார்

5. புறநானூறு
- சிறுவனே வள்ளலானான்

6. அகநானூறு (4) - வண்டு
நற்றிணை (11) - நண்டு
கலித்தொகை (11) - யானை, புறா
ஐந்திணை 50 (27) - மான்

ஆகியவை பற்றிய செய்திகள்

UNIT V **நவீன தமிழ் இலக்கியம்** **6**

1. உரைநடைத் தமிழ்,
- தமிழின் முதல் புதினம்,
- தமிழின் முதல் சிறுகதை,
- கட்டுரை இலக்கியம்,
- பயண இலக்கியம்,
- நாடகம்,

2. நாட்டு விடுதலை போராட்டமும் தமிழ் இலக்கியமும்,
3. சமுதாய விடுதலையும் தமிழ் இலக்கியமும்,
4. பெண் விடுதலையும் விளிம்பு நிலையினரின் மேம்பாட்டில் தமிழ்

இலக்கியமும்,

5. அறிவியல் தமிழ்,
6. இணையத்தில் தமிழ்,
7. சுற்றுச் சூழல் மேம்பாட்டில் தமிழ் இலக்கியம்.

TOTAL: 30 PERIODS

<u>தமிழ் இலக்கிய வெளியீடுகள் / புத்தகங்கள்</u>

1. தமிழ் இணைய கல்விக்கழகம் (Tamil Virtual University)
   - www.tamilvu.org
2. தமிழ் விக்கிப்பீடியா (Tamil Wikipedia)
   -https://ta.wikipedia.org
3. தர்மபுர ஆதீன வெளியீடு
4. வாழ்வியல் களஞ்சியம்
   - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்
5. தமிழ்கலைக் களஞ்சியம்
   - தமிழ் வளர்ச்சித்துறை (thamilvalarchithurai.com)
6. அறிவியல் களஞ்சியம்
   - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்