ANNA UNIVERSITY, CHENNAI
NON - AUTONOMOUS COLLEGES AFFILIATED ANNA UNIVERSITY
M.E. VLSI DESIGN AND EMBEDDED SYSTEMS
REGULATIONS – 2021
CHOICE BASED CREDIT SYSTEM

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):

1. To enrich students in the cutting edge technologies of VLSI design and Embedded systems and create competent professionals and researchers in this field
2. To provide students with a good foundation in computer architecture principles and digital systems design as these areas are vital for the VLSI design industry
3. To understand the various applications and employ embedded systems to find solutions to them with good scientific and engineering knowledge so as to comprehend, analyze, design, and create novel products and solutions for the real life problems.
4. To provide students with an academic environment aware of excellence, leadership, ethical conduct, positive attitude, societal responsibilities and the lifelong learning needed for a successful professional career.
5. To inculcate entrepreneurial skills in setting startups serving the needs of the industry sectors that depend on VLSI design and Embedded Systems.

PROGRAM OUTCOMES (POs)

1. An ability to independently carry out research/investigation and development work to solve practical problems
2. An ability to write and present a substantial technical report/document
   Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
3. Master the fundamentals, associated with the different specializations of VLSI and Embedded systems domain.
4. Provide solutions through research to the social relevant issues with the knowledge, techniques, skills in VLSI and Embedded systems domain using the required hardware and modern tools for the benefit of the society.
5. Pursue a successful research career in VLSI and Embedded systems field or take on challenging assignments in the industry.
### Semester I

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## PROFESSIONAL ELECTIVES

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## RESEARCH METHODOLOGY AND IPR COURSES (RMC)

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## EMPLOYABILITY ENHANCEMENT COURSES (EEC)

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### SUMMARY

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COURSE OBJECTIVES:

- To introduce graph as mathematical model to solve connectivity related problems.
- To introduce fundamental graph algorithms.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in real life situation.
- To provide knowledge and training using non-linear programming under limited resources for the engineering and business problems.
- To understand the applications of simulation modelling in engineering problems.

UNIT I  GRAPHS  12
Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

UNIT II  GRAPH ALGORITHM  12
Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

UNIT III  LINEAR PROGRAMMING  12

UNIT IV  NON-LINEAR PROGRAMMING  12

UNIT V  SIMULATION MODELLING  12

TOTAL : 60 PERIODS

COURSE OUTCOMES:
At the end of the course, students will be able to
1. apply graph ideas in solving connectivity related problems.
2. apply fundamental graph algorithms to solve certain optimization problems.
3. formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
4. model various real life situations as optimization problems and effect their solution through Non-linear programming.
5. apply simulation modeling techniques to problems drawn from industry management and other engineering fields.

REFERENCES:

RM4151 RESEARCH METHODOLOGY AND IPR

UNIT I RESEARCH DESIGN
Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

UNIT II DATA COLLECTION AND SOURCES
Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods.
Data - Preparing, Exploring, examining and displaying.

UNIT III DATA ANALYSIS AND REPORTING
Overview of Multivariate analysis, Hypotheses testing and Measures of Association.
Presenting Insights and findings using written reports and oral presentation.

UNIT IV INTELLECTUAL PROPERTY RIGHTS

UNIT V PATENTS

TOTAL:30 PERIODS

REFERENCES:
COURSE OBJECTIVES:
- Analog Circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology. The most important building blocks of all CMOS analog IC will be the topic of study in this course.
- The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.
- The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.

UNIT I SINGLE STAGE AMPLIFIERS
Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

UNIT II HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS
Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.

UNIT III FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS
Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER
Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage And Using Cascode Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, And Compensation Of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.

UNIT V BANDGAP REFERENCES
Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascode current source, design of high swing cascode sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing.

COURSE OUTCOMES:
At the end of this course, the students will be able to:

CO1: Design amplifiers to meet user specifications
CO2: Analyse the frequency and noise performance of amplifiers
CO3: Design and analyse feedback amplifiers and one stage op amps
CO4: Design and analyse two stage op amps
CO5: Design and analyse current mirrors and current sinks with mos devices

TOTAL: 45 PERIODS

REFERENCES:
5. Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320_2021/start

VL4152 DIGITAL CMOS VLSI DESIGN

COURSE OBJECTIVES:
- To introduce the transistor level design of all digital building blocks common to all cmos microprocessors, network processors, digital backend of all wireless systems etc.
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER
MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, Elmore constant, CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.

UNIT II COMBINATIONAL LOGIC CIRCUITS
Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS
Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS
Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.

UNIT V MEMORY ARCHITECTURES
Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.

COURSE OUTCOMES:
At the end of this course, the students will be able to:
CO1: Use mathematical methods and circuit analysis models in analysis of CMOS digital circuits

10
CO2: Create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort
CO3: Design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches
CO4: Understand design methodology of arithmetic building blocks
CO5: Design functional units including ROM and SRAM

TOTAL: 45 PERIODS

REFERENCES:

VE4151 EMBEDDED CONTROLLERS L T P C 3 0 0 3

COURSE OBJECTIVES:
- To study the architecture and programming of PIC microcontrollers.
- To learn interfacing with PIC microcontrollers.
- To understand the ARM processor architecture.
- To program using ARM Instruction Set.
- To design and develop embedded applications.

UNIT I PIC MICROCONTROLLER – ARCHITECTURE 9
RISC Vs CISC Architectures – PIC Architecture and Assembly Language Programming - Program Memory Organization- Branch, Call and Time Delay Loop - PIC I/O Port Programming - Arithmetic and Logic Instructions and Programs - PIC Bank Switching, Table Processing, Macros And Modules PIC Configuration Registers-PIC Hardware Connection-ROM Loaders.

UNIT II PIC INTERFACING 9
PIC Timer / Counter Programming - Timers 0 And 1- Programming Timers 2 and 3 -Serial Port Programming -Interrupt Programming -Flash / EEPROM Programming - Standard and Enhanced CCP Modules -Compare Mode Programming - Capture Mode Programming- PWM Programming- ECCP Programming.

UNIT III ARM ARCHITECTURE 9
UNIT IV  ARM PROGRAMMING

ARM Instruction Set - Data Processing Instructions – Branch Instructions — Load Store Instructions – Software Interrupt Instruction – Program Status Register Instructions – Conditional Execution - Thumb Instruction Set-Thumb Programmers Model-Thumb Branch Instructions- Thumb Data Processing Instructions-Thumb Single Register Data Transfer- Thumb Multiple Register Data Transfer Instructions - Thumb Implementation.

UNIT V  EMBEDDED APPLICATIONS


SUGGESTED ACTIVITIES:
1: Interfacing PIC microcontrollers with peripherals.
2: Assignments on programming ARM processors.
3: Design embedded systems for real – time applications.

COURSE OUTCOMES:
CO1: Understand the architecture of a PIC microcontroller.
CO2: Program using PIC microcontrollers.
CO3: Program using ARM processors.
CO4: Design interfacing circuits with PIC microcontrollers.
CO5: Design embedded applications to solve real world problems.

REFERENCES:

VE4152  EMBEDDED SYSTEM DESIGN  L T P C
3 0 0 3

COURSE OBJECTIVES:
- To understand the design challenges in embedded systems.
- To program the Application Specific Instruction Set Processors.
- To understand the bus structures and protocols.
- To model processes using a state – machine model.
- To design a real time embedded system.

UNIT I  EMBEDDED SYSTEM OVERVIEW

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom
Components, Optimizing Custom Single-Purpose Processors.

UNIT II  GENERAL AND SINGLE PURPOSE PROCESSOR  

UNIT III  BUS STRUCTURES  

UNIT IV  STATE MACHINE AND CONCURRENT PROCESS MODELS  

UNIT V  SYSTEM DESIGN  
Burglar alarm system-Design goals -Development strategy-Software development-Relevance to more complex designs- Need for emulation -Digital echo unit-Creating echo and reverb-Design requirements-Designing the codecs -The overall system design

SUGGESTED ACTIVITIES:  
1: Do microcontroller based design experiments.  
2: Create program –state models for different embedded applications.  
3: Design and develop embedded solutions for real world problems.

COURSE OUTCOMES:  
CO1: Knowledge of different protocols  
CO2: Apply state machine techniques and design process models.  
CO3: Apply knowledge of embedded software development tools and RTOS  
CO4: Apply networking principles in embedded devices.  
CO5: Design suitable embedded systems for real world applications.

TOTAL: 45 PERIODS

REFERENCES:  
COURSE OBJECTIVES:

- To interface sensors and display devices with microcontroller.
- To program timers and UART in a microcontroller.
- To understand I2C and CAN protocols.
- To understand concepts of scheduling, semaphores and deadlocks using RTOS.
- To design a real – time data acquisition system.

LIST OF EXPERIMENTS:

1: Interfacing sensors and actuators with microcontroller.
2: Configuration and programming timers and UART in microcontroller.
3: Interfacing LCD and OLED display modules with microcontroller.
4: Simulation of I2C and CAN protocols.
5: Simple task scheduling using freeware RTOS.
6: Exploration on semaphores, deadlocks using RTOS.
7: Exploration of any one SOC architecture using RTOS.
8: Study of Edge AI platform on any one of the embedded processors.
9: Design of a real – time data acquisition system and control using a microcontroller.
10. Design of an IoT based system.

HARDWARE/SOFTWARE REQUIREMENTS

1: Any microcontroller
2: RTOS Freeware

COURSE OUTCOMES:

CO1: Interface a microcontroller with input – output devices.
CO2: Understand I2C and CAN protocols.
CO3: Explore concepts in RTOS.
CO4: Design a real – time embedded system.
CO5: Analyse design requirements of an IoT based system.

REFERENCES

VE4112  ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY  

COURSE OBJECTIVES:
- To learn the principles of CMOS amplifiers
- To design single stage and multistage amplifiers and their design constrains
- To learn Hardware Descriptive Language (Verilog/VHDL)
- To learn the fundamental principles of VLSI circuit design in digital domain
- To familiarize programming on FPGAs
- To understand the critical design issues of digital logic design

LIST OF EXPERIMENTS:
Part I: Module Design and Simulation using SPICE simulator
1. Design of Common Source Amplifier
2. Design of Cascade and Cascode amplifiers
3. Design of current Mirrors
4. Design of differential pair amplifier with active load
5. Design of telescopic amplifier circuit
6. Design of two-stage amplifier circuit

Part II: Module Design using FPGA Implementation (Verilog/VHDL):
1. Adders and Subtractors
2. Multiplier (8-bit)
3. ALU circuit
4. Flip-flops
5. Universal Shift Registers
6. Asynchronous and synchronous Counters
7. Finite State Machine (Moore/Mealy) and its applications
8. Memories

TOTAL: 60 PERIODS

COURSE OUTCOMES:
On successful completion of this course, students will be able to

CO1: Design digital and analog Circuit using CMOS given a design specification.
CO2: Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances
CO3: Use EDA tools for Circuit Design

VL4251  DESIGN FOR VERIFICATION USING UVM  

COURSE OBJECTIVES:
- To provide the students complete understanding on UVM testing
- To become proficient at UVM verification,
- To provide an experience on self checking UVM testbenches
UNIT I  INTRODUCTION  9
Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation

UNIT II  DEVELOPING REUSABLE VERIFICATION COMPONENTS  9
Modeling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage

UNIT III  UVM USING VERIFICATION COMPONENTS  9
Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes - Verification Component Configuration - Creating and Selecting a User-Defined Test - Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards- Implementing a Coverage Model

UNIT IV  UVM USING THE REGISTER LAYER CLASSES  9
Using The Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register-Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre-Defined Sequences

UNIT V  ASSIGNMENT IN TESTBENCHES  9
Assignment, APB: Protocol, Test bench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module. TOTAL: 45 PERIODS

COURSE OUTCOMES:
At the end of the course, students will be able to
CO1:understand the basic concepts of two methodologies UVM
CO2:build actual verification components.
CO3:generate the register layer classes.
CO4:code testbenches using UVM.
CO5:understand advanced peripheral bus testbenches.

REFERENCES
5. http://www.testbench.in/ot_00_index.html
COURSE OBJECTIVES:
- Students can understand the concepts of FPGA and the need for FPGA in embedded.
- The course is to provide a thorough understanding about and hands-on practice with FPGA based digital system design and emulation.
- To make the student learn, FPGA fundamentals, design and implementation of Circuits In Them.
- Understanding the Role of FPGAs and ASIC In Embedded Systems.

UNIT I  FPGA ARCHITECTURE AND OVERVIEW  9

UNIT II  EMBEDDED SYSTEM DESIGN  9

UNIT III  VERILOG CONSTRUCTS  9
VLSI Design Flow- Behavioral Style, the Dataflow Style, And Structural Style - Data Types - Constants - Assignment Statement - Operators - Conditional Expressions – Statement Types - Vector Operations – Bit Selects - Functions - Gate Level Modeling.

UNIT IV  VERILOG MODELING COMBINATIONAL CIRCUITS  9
Combinational Logic -Adders - Multiplexers - Decoders -Comparator -Parity Generators ALU – Three State Gate - UART Model.

UNIT V  VERILOG MODELLING SEQUENTIAL CIRCUITS  9

TOTAL: 45 PERIODS

PRACTICAL EXERCISES:  30 PERIODS
1. Design Entry Using VHDL Or Verilog Using HDL Languages of
   I. Combinational Circuits Namely 8:1 Mux/Demux, Full Adder, 8-Bit Magnitude Comparator, Encoder/Decoder, Priority Encoder.
   II. Sequential Circuits Namely D-FF, 4-Bit Shift Registers (SISO, SIPO, PISO, Bidirectional), 3-Bit Synchronous Counters.
2. Test Vector Generation And Timing Analysis of Sequential And Combinational Logic Design for exercise (1) above.
4. FPGA Implementation of PCI Bus & Arbiter.
5. Verifying Design Functionality Using Either Chipscope Feature (Xilinx) /the Signal Tap Feature (Altera)/Other Equivalent Feature. Invoke the PLL And Demonstrate the Use of the PLL Module for Clock Generation in FPGAs.

**TOTAL:45+30=75 PERIODS**

**COURSE OUTCOMES:**

**CO1:** students can learn the concepts of FPGA.

**CO2:** students can design embedded system with appropriate FPGA based on applications

**CO3:** students can write verilog code for combinational and sequential logics

**CO4:** students can design a combinational circuit using Verilog.

**CO5:** students can use FPGA EDA tools for design and analysis.

**REFERENCES**


**VE4202**

**EMBEDDED AUTOMATION**

**LTPC**

3 0 0 3

**COURSE OBJECTIVES:**

- To learn about the process involved in the design and development of real-time embedded system
- To develop the embedded C programming skills on 8-bit microcontroller
- To study about the interfacing mechanism of peripheral devices with 8-bit microcontrollers
- To learn about the tools, firmware related to microcontroller programming
- To build a home automation system

**UNIT - I**

**INTRODUCTION TO EMBEDDED C PROGRAMMING**

C Overview and Program Structure - C Types, Operators and Expressions - C Control Flow - C Functions and Program Structures - C Pointers And Arrays - FIFO and LIFO - C Structures - Development Tools
UNIT - II  AVR MICROCONTROLLER  
ATMEGA 16 Architecture - Nonvolatile and Data Memories - Port System - Peripheral Features : Time Base, Timing Subsystem, Pulse Width Modulation, USART, SPI, Two Wire Serial Interface, ADC, Interrupts - Physical and Operating Parameters

UNIT – III  HARDWARE AND SOFTWARE INTERFACING WITH 8-BIT SERIES CONTROLLERS  
Lights and Switches - Stack Operation - Implementing Combinational Logic - Expanding I/O - Interfacing Analog To Digital Convertors - Interfacing Digital To Analog Convertors - LED Displays : Seven Segment Displays, Dot Matrix Displays - LCD Displays - Driving Relays - Stepper Motor Interface - Serial EEPROM - Real Time Clock - Accessing Constants Table - Arbitrary Waveform Generation - Communication Links - System Development Tools

UNIT – IV  VISION SYSTEM  

UNIT – V  HOME AUTOMATION  
Home Automation - Requirements - Water Level Notifier - Electric Guard Dog - Tweeting Bird Feeder - Package Delivery Detector - Web Enabled Light Switch - Curtain Automation - Android Door Lock - Voice Controlled Home Automation - Smart Lighting - Smart Mailbox - Electricity Usage Monitor - Proximity Garage Door Opener - Vision Based Authentic Entry System

TOTAL: 45 PERIODS

COURSE OUTCOMES:  
On successful completion of this course, students will be able to  
CO1: analyze the 8-bit series microcontroller architecture, features and pin details  
CO2: write embedded C programs for embedded system application  
CO3: design and develop real time systems using AVR microcontrollers  
CO4: design and develop the systems based on vision mechanism  
CO5: design and develop a real time home automation system

REFERENCES:  
VE4203  VLSI STRUCTURES FOR DSP   L T P C  3 0 0 3

COURSE OBJECTIVES:
- To Understand the Fundamentals of DSP
- To Learn Various DSP Structures And Their Implementation.
- To Know Designing Constraints of Various Filters
- Design And Optimize VLSI Architectures for Basic DSP Algorithms
- To Enable Students To Design VLSI System With High Speed And Low Power.

UNIT I  INTRODUCTION TO DIGITAL SIGNAL PROCESSING  9
Linear System Theory- Convolution- Correlation - DFT- FFT- Basic Concepts In FIR Filters And IIR Filters- Filter Realizations. Representation of DSP Algorithms-Block Diagram-SFG-DFG.

UNIT II  ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER  9

UNIT III  RETIMING, UNFOLDING AND FOLDING  9

UNIT IV  FAST CONVOLUTION  9
Cook-Toom Algorithm- Modified Cook-Toom Algorithm. Design of Fast Convolution Algorithm By Inspection

UNIT V  ARITHMETIC STRENGTH REDUCTION IN FILTERS  9

TOTAL:45 PERIODS

COURSE OUTCOMES:
At the end of the course student will be able
CO1: acquired knowledge about fundamentals of DSP processors.
CO2: improve the overall performance of DSP system through various transformation and optimization techniques.
CO3: foster ability to understand the need of different types of instructions for DSP.
CO4: optimize design in terms of computation complexity and speed.
CO5: understand clock based issues and design asynchronous and wave pipelined systems.

REFERENCES
COURSE OBJECTIVES:

- the course enables student to understand the basics of Internet of Things and protocols
- This program aims to train students to be equipped with a solid theoretical foundation, systematic professional knowledge and strong practical skills in the IoT platform and system design.
- the course focuses on understanding the vision of IoT from a global perspective, understand its applications, determine its market perspective, using gateways, devices and data management
- To understand the concepts behind building a state of art architecture in IoT.
- the course focuses on applications in commercial building automation and real world design constraints

UNIT I  IOT NETWORKING CORE  9
Technologies Involved In IoT Development, Internet Web And Networking Technologies, Infrastructure, Overview of IoT Supported Hardware Platforms Such As: Raspberry Pi, ARM Cortex Processors, Arduino and Intel Galileo Boards, Wireless Networking Equipment and Configurations, Accessing Hardware and Device File Interactions

UNIT II  M2M TO IOT  9
Role of M2M In IoT, M2M Value Chains, IoT Value Chains, An Emerging Industrial Structure for IoT, the International Driven Global Value Chain And Global Information Monopolies. Building Architecture, Main Design Principles and Needed Capabilities, An IoT Architecture Outline, Standards Considerations.

UNIT III  IOT ARCHITECTURE -STATE OF THE ART  9

UNIT IV  IOT APPLICATION DEVELOPMENT  9
Application Protocols: MQTT, Rest/Http, COAP, MYSQL, Back-End Application Designing Apache for Handling Http Requests, MONGODB Object Type Database, HTML, CSS & JQUERY for UI Designing, JSON Lib for Data Processing, Security & Privacy During Development

UNIT V  IOT SECURITY AND CASE STUDIES  9

TOTAL:45 PERIODS
COURSE OUTCOMES
At the end of this course, the students should will be able to:
CO1: study of basic structure lying in IoT
CO2: understand challenges in Internet of Things (IoT) system design
CO3: understand distributed embedded system hardware.
CO4: understand specifications and modeling approaches for real-time and IoT systems
CO5: obtain knowledge of IoT applications

REFERENCES

VE4211 TERM PAPER WRITING AND SEMINAR

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (atleast 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing each paper.
6. Preparing a working outline
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.
Activities to be carried out

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<th>Activity</th>
<th>Instructions</th>
<th>Submission week</th>
<th>Evaluation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Selection of area of interest</td>
<td>You are requested to select an area of interest, topic and state an objective</td>
<td>2nd week</td>
<td>3 % Based on clarity of thought, current relevance and clarity in writing</td>
</tr>
<tr>
<td>and Topic</td>
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<tr>
<td>Stating an Objective</td>
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</tbody>
</table>
| Collecting Information about your area & topic | 1. List 1 Special Interest Groups or professional society  
2. List 2 journals  
3. List 2 conferences, symposia or workshops  
4. List 1 thesis title  
5. List 3 web presences (mailing lists, forums, news sites)  
6. List 3 authors who publish regularly in your area  
7. Attach a call for papers (CFP) from your area. | 3rd week | 3%  
( the selected information must be area specific and of international and national standard) |
| Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter | • You have to provide a complete list of references you will be using - Based on your objective - Search various digital libraries and Google Scholar  
• When picking papers to read - try to:  
  • Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them,  
  • Favour papers from well-known journals and conferences,  
  • Favour “first” or “foundational” papers in the field (as indicated in other people’s survey paper),  
  • Favour more recent papers,  
  • Pick a recent survey of the field so you can quickly gain an overview,  
  • Find relationships with respect to each other and to your topic area (classification scheme/categorization)  
• Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered | 4th week | 6%  
( the list of standard papers and reason for selection) |
| Reading and notes for first 5 papers | Reading Paper Process  
• For each paper form a Table answering the following questions:  
  • What is the main topic of the article?  
  • What was/were the main issue(s) the author said they want to discuss?  
  • Why did the author claim it was important?  
  • How does the work build on other’s work, in the author’s opinion? | 5th week | 8%  
( the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper) |
<p>| Reading and notes for next 5 papers | Repeat Reading Paper Process | 6th week | 8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper) |
| Reading and notes for final 5 papers | Repeat Reading Paper Process | 7th week | 8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper) |
| Draft outline 1 and Linking papers | Prepare a draft Outline, your survey goals, along with a classification / categorization diagram | 8th week | 8% (this component will be evaluated based on the linking and classification among the papers) |
| Abstract | Prepare a draft abstract and give a presentation | 9th week | 6% (Clarity, purpose and conclusion) 6% Presentation &amp; Viva Voce |
| Introduction Background | Write an introduction and background sections | 10th week | 5% (clarity) |
| Sections of the paper | Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey | 11th week | 10% (this component will be evaluated based on the linking and classification among the papers) |</p>
<table>
<thead>
<tr>
<th>Task</th>
<th>Description</th>
<th>Week</th>
<th>Weight</th>
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</thead>
<tbody>
<tr>
<td>Your conclusions</td>
<td>Write your conclusions and future work</td>
<td>12th</td>
<td>5%</td>
</tr>
<tr>
<td>Final Draft</td>
<td>Complete the final draft of your paper</td>
<td>13th</td>
<td>10%</td>
</tr>
<tr>
<td>Seminar</td>
<td>A brief 15 slides on your paper</td>
<td>14th &amp; 15th</td>
<td>10%</td>
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**TOTAL: 30 PERIODS**

**VE4212 EMBEDDED AUTOMATION LABORATORY**

**COURSE OBJECTIVES:**
- To learn about the design and development of different automation systems
- To enhance the embedded C programming skills
- To study about the interfacing mechanism of peripheral devices with microcontrollers
- To improve the programming skills related to computer vision
- To build a home automation system

**LIST OF EXPERIMENTS:**
1. Water level controller
2. Unauthorized entry identifier
3. Tweeting bird feeder
4. Package delivery detector
5. Web enabled light switch
6. Curtain automation
7. Android door lock
8. Voice controlled home automation
9. Smart lighting
10. Smart mailbox
11. Proximity garage door opener
12. Wi Fi Managed Vehicle Parking and Theft Control

**TOTAL: 60 PERIODS**

**COURSE OUTCOMES:**
On successful completion of this course, students will be able to
**CO1:** design and develop real time systems using microcontrollers
**CO2:** design and develop the systems based on vision mechanism
**CO3:** to be able to build large, complex systems
**CO4:** design and develop a real time home automation system
**CO5:** students should be able to know the different embedded tools
VL4071  ASIC DESIGN  L T P C  3 0 0 3

COURSE OBJECTIVES:

- To Focus on the Semi-Custom IC Design and introduces the Principles of Design Logic Cells, I/O Cells and Interconnect Architecture, with Equal Importance given to FPGA and ASIC styles.

- To deal with the entire FPGA and ASIC Design Flow from the Circuit and Layout Design Point of View

UNIT I  INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN  9

Types of Asics - Design Flow - CMOS Transistors - Combinational Logic Cell – Sequential Logic Cell - Data Path Logic Cell - Transistors as Resistors - Transistor Parasitic Capacitance - Logical Effort.

UNIT II  PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS  9

Anti Fuse - Static Ram - EPROM and EEPROM Technology - ACTEL ACT- Xilinx LCA – ALTERA FLEX - ALTERA MAX DC & AC Inputs and Outputs - Clock & Power Inputs - Xilinx I/O Blocks.

UNIT III  PROGRAMMABLE ASIC ARCHITECTURE  9


UNIT IV  LOGIC SYNTHESIS, PLACEMENT AND ROUTING  9


UNIT V  SYSTEM-ON-CHIP DESIGN  9

SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators. Case Studies: Digital Camera, SDRAM, High Speed Data standards.

TOTAL :45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be

CO1: able to apply Logical Effort Technique for predicting Delay, Delay Minimization and FPGA Architectures

CO2: able to Design Logic Cells and I/O Cells

CO3: able to analyze the various resources of recent FPGAs

CO4: able to use Algorithms for Floor Planning and Placement of Cells and to Apply Routing Algorithms for Optimization of Length and Speed.

CO5: able to analyze High Performance Algorithms Available for ASICs
REFERENCES

VE4001 PARALLEL AND RECONFIGURABLE ARCHITECTURES

COURSE OBJECTIVE:
- To Educate the Students to the Fundamentals of Parallel Processing
- To Teach the Fundamentals of Network Topologies for Multiprocessors
- To Introduce Different Pipeline Designs
- To Introduce Features of Parallel Processors, Memory Technologies, OS for Multi-programmed Computer
- To Involve Discussions/ Practice/Exercise Onto Revising & Familiarizing the Concepts Acquired Over the 5 Units of the Subject for Improved Employability Skills

UNIT - I THEORY OF PARALLELISM

UNIT - II SYSTEM INTERCONNECT ARCHITECTURES

UNIT – III PIPELINING AND SUPERSCALAR TECHNOLOGIES
Pipeline Principle and Implementation - Classification of Pipeline Processor - Introduction of Arithmetic, Instruction, Processor Pipelining - Pipeline Mechanisms - Hazards.

UNIT – IV HARDWARE TECHNOLOGIES

UNIT – V OS ISSUES FOR MULTI PROCESSOR
Introduction - Need for Preemptive OS – Synchronising and Scheduling in Multiprocessor OS-, usual OS Scheduling Techniques, Threads – Classification of Multiprocessor OS – Software Requirements of Multiprocessor OS, Distributed Scheduler – PVM – PT Threads in Shared Memory Systems.

TOTAL: 45 PERIODS
COURSE OUTCOMES:
At the end of this course, the students will be
CO1: Able to understand the operations of Multiprocessor and Multicomputer Systems.
CO2: Able to understand the various Advanced Processor Technology, Pipelining and Scalable Architectures.
CO3: Able to know the working of Superscalar Pipeline, Cache Memory Organization.
CO4: Able to understand the principles of Multithreading, Multi Thread Architecture, Static and Dynamic Dataflow.
CO5: To improve employability and entrepreneurship capacity due to knowledge upgradation on recent trends in Embedded Systems Design.

REFERENCES

VE4002 SOFTWARE FOR EMBEDDED SYSTEMS

COURSE OBJECTIVES:
• To Expose the Students to the fundamentals of Embedded Programming
• To introduce the GNU C Programming Tool Chain in Linux.
• To study the basic Concepts of Embedded C.
• To teach the basics of Python Programming
• To involve Discussions/ Practice/Exercise onto Revising & familiarizing the concepts acquired over the 5 units of the subject for Improved Employability Skills.

UNIT I BASIC C PROGRAMMING
Typical C Program Development Environment - Introduction to C Programming – Structured Program Development in C - Data Types and Operators - C Program Control - C Functions - Introduction to Arrays.

UNIT II EMBEDDED C

UNIT III C PROGRAMMING TOOL-CHAIN IN LINUX
C Preprocessor - Stages of Compilation - Introduction to GCC - Debugging with GDB - the Make Utility - GNU Configure and Build System - GNU Binary Utilities - Profiling - Using GPROF - Introduction to GNU C Library.
UNIT IV  PYTHON PROGRAMMING  9
Introduction - Parts of Python Programming Language - Control Flow Statements - Functions - Strings - Lists - Dictionaries - Tuples and Sets.

UNIT V  MODULES, PACKAGES AND LIBRARIES IN PYTHON  9

TOTAL:45 PERIODS

COURSE OUTCOMES:
At the end of this course, the students will be
CO1: able to understand C Programming and its Salient Features for Embedded Systems
CO2: able to learning Process Delivers Insight Into Various Programming Languages/Software Compatible to Embedded Process Development with Improved Design & Programming Skills.
CO3: able to develop knowledge on C Programming in Linux environment.
CO4: able to write Python Programming for Embedded applications.
CO5: able to improve Employability and Entrepreneurship Capacity due to knowledge upgradation on recent trends in Embedded Programming Skills.

REFERENCES

VE4003  EMBEDDED SYSTEM SECURITY  L T P C
3 0 0 3

COURSE OBJECTIVES:
- To learn Cryptographic Concepts in the Context of Embedded Systems and their Unique Constraints and Requirements.
- To expose Forensics Procedures and Digital Data Acquisition Mechanisms using FKT and FRED

UNIT I  INTRODUCTION  9
UNIT II EMBEDDED CRYPTOGRAPHY

UNIT III EMBEDDED SYSTEMS SECURITY REQUIREMENTS AND ISSUES

UNIT IV DIGITAL FORENSICS

UNIT V PRACTICE WITH FORENSIC TOOLS
Data Acquisition Hardware Tools, Use Fred to Create Images on Different Media, Recovering the Deleted Files, Investigative Tools (Open Source and Proprietary), Using Forensic Software Such as FTK/Encase Etc. Use FTK Preview Evidence, Export Evidence Files, Create Forensic Images and Convert Existing Images, Create a Case in FTK, Use FTK to Process and Analyze Documents, Metadata, Graphics and E-Mail, Use the FTK Data Carving Feature to Recover Files from Unallocated Disk Space. Web/E-Mail Forensics analysis, Mobile Evidence, Extracting and Analysing Mobile Evidence.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
At the end of the course, students will demonstrate the ability to:

CO1: Recognize vulnerabilities, attacks and need of protection mechanisms for embedded systems

CO2: Analyze and evaluate software vulnerabilities and attacks on Operating Systems

CO3: Identify terms/concepts relevant to Embedded Cryptography

CO4: Develop and deploy solutions for Security of Embedded Software and Data Protection

REFERENCES
5. CEH: Certified Ethical Hacker Version 8 Study Guide By Sean-Philip Oriyano (Author) Publisher Sybex, 2014
<table>
<thead>
<tr>
<th>COURSE OBJECTIVES:</th>
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<tbody>
<tr>
<td>• to introduce the VLSI testing.</td>
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<tr>
<td>• to introduce logic and fault simulation and testability measures</td>
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<td>• to study the test generation for combinational and sequential circuits</td>
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<td>• to study the design for testability.</td>
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<td>• to study the fault diagnosis</td>
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<tr>
<th>UNIT I</th>
<th>INTRODUCTION TO TESTING</th>
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<tr>
<th>UNIT II</th>
<th>LOGIC &amp; FAULT SIMULATION &amp; TESTABILITY MEASURES</th>
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<tr>
<th>UNIT III</th>
<th>TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS</th>
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<tr>
<th>UNIT IV</th>
<th>DESIGN FOR TESTABILITY</th>
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<tr>
<th>UNIT V</th>
<th>FAULT DIAGNOSIS</th>
<th>9</th>
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<tbody>
<tr>
<td>Introduction and Basic Definitions – Fault Models for Diagnosis – Generation of Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.</td>
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| TOTAL:45 PERIODS |

<table>
<thead>
<tr>
<th>COURSE OUTCOMES:</th>
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<tbody>
<tr>
<td>At the end of this course, the students should will be able to:</td>
</tr>
<tr>
<td>CO1: Understand VLSI Testing Process</td>
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<tr>
<td>CO2: Develop Logic Simulation and Fault Simulation</td>
</tr>
<tr>
<td>CO3: Develop Test for Combinational and Sequential Circuits</td>
</tr>
<tr>
<td>CO4: Understand the Design for Testability</td>
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<tr>
<td>CO5: Perform Fault Diagnosis.</td>
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<table>
<thead>
<tr>
<th>REFERENCES</th>
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</table>
COURSE OBJECTIVES:
The students should be made to:
- Understand the concept of Network - on - Chip
- Learn router architecture designs
- Study fault tolerance Network - on – Chip

UNIT I INTRODUCTION TO NOC
Introduction to NOC – OSI Layer Rules in NOC - Interconnection Networks in Network-On-Chip
Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support

UNIT II ARCHITECTURE DESIGN

UNIT III ROUTING ALGORITHM

UNIT IV TEST AND FAULT TOLERANCE OF NOC
Design-Security in Networks-On-Chips-Formal Verification of Communications in Networks-On Chips-Test and Fault Tolerance For Networks-On-Chip Infrastructures-Monitoring Services For Networks-On-Chips

UNIT V THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP

COURSE OUTCOMES:
At the end of this course, the students will be able to:
CO1: Compare different architecture design
CO2: Discuss different routing algorithms
CO3: Explain three dimensional Networks on Chip architectures
CO4: Test and design fault tolerant NOC
CO5: Design three dimensional architectures of NOC

REFERENCES


VL4074 NANOTECHNOLOGY

COURSE OBJECTIVES:
- Provides knowledge of various industrial applications of Nanotechnology
- Introduces the theory and practice on Nanomaterials
- Imparting the state of art of nanotechnology to the society and to the environmental implication
- To exercise the students’ knowledge and imagination of Nanoscience and nanotechnology toward engineering applications coupled with detailed justifications.

UNIT I NANOTECHNOLOGY
Background, what is Nanotechnology, types of Nanotechnology and Nano-machines, top down and bottom up techniques, atomic manipulation-Nanodots, semi-conductor quantum dots, self-assembly monolayers, simple details of characterization tools- SEM, TEM, STM, AFM.

UNIT II NANOMATERIALS
What are Nanomaterials? Preparation of Nanomaterials- solid state reaction method, Chemical Vapor Deposition, SOL-GELS techniques, electrodeposition, ball milling, introduction to lithography, Pulse Laser Deposition (PLD), applications of Nanomaterials

UNIT III CARBON TUBES
New forms of carbon, carbon tubes-types of Nanotubes, formation of Nanotubes, assemblies, purification of carbon Nanotubes, properties of Nanotubes, applications of Nanotubes

UNIT IV OPTICS, PHOTONICS AND SOLAR ENERGY
Light and Nanotechnology, interaction of light and Nanotechnology, Nanoholes and photons, solar cells, optically useful Nanostructured polymers, photonic crystals.

UNIT V FUTURE APPLICATIONS
MEMS, Nanomachines, Nanodevices, Quantum Computers, Opto-electronic Devices, Quantum Electronic devices, environmental and biological applications.

TOTAL:45 PERIODS

COURSE OUTCOMES:
At the end of this course, the students should will be able to:

CO1: understand the bases for introduction to Nanotechnology
CO2: understand the synthesis of Nanomaterials and their application and the impact of Nanomaterials on environment
CO3: acquire knowledge about various kind of Nano materials
CO4: understand the Nanotechnology devices used and their structures
CO5: understand and improve the application of Nanotechnology
REFERENCES

VL4291 LOW POWER VLSI DESIGN L T P C 3 0 0 3

COURSE OBJECTIVES:
- identify sources of power in an IC.
- identify the power reduction techniques based on technology independent and technology dependent methods
- identify suitable techniques to reduce the power dissipation
- estimate power dissipation of various MOS logic circuits
- develop algorithms for low power dissipation

UNIT I POWER DISSIPATION IN CMOS 9

UNIT II POWER OPTIMIZATION 9
Logic Level Power Optimization – Circuit Level Low Power Design – Gate Level Low Power Design –Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

UNIT IV POWER ESTIMATION 9
Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER CMOS CIRCUITS 9

TOTAL:45 PERIODS
COURSE OUTCOMES:
At the end of this course, the students should will be able to:
CO1: able to find the power dissipation of MOS circuits
CO2: design and analyze various MOS logic circuits
CO3: apply low power techniques for low power dissipation
CO4: able to estimate the power dissipation of ICs
CO5: able to develop algorithms to reduce power dissipation by software.

REFERENCES

VE4004 MULTICORE ARCHITECTURE PROGRAMMING

OBJECTIVES:
• Understand the challenges in parallel and multi-threaded programming.
• Learn about the various parallel programming paradigms, and solutions.

UNIT I MULTI-CORE PROCESSORS
Single Core To Multi-Core Architectures – SIMD And MIMD Systems – Interconnection Networks - Symmetric And Distributed Shared Memory Architectures – Cache Coherence - Performance Issues –Parallel Program Design

UNIT II PARALLEL PROGRAM CHALLENGES
Performance – Scalability – Synchronization And Data Sharing – Data Races – Synchronization Primitives (_mutexes, Locks, Semaphores, Barriers) – Deadlocks And Livelocks – Communication Between Threads (Condition Variables, Signals, Message Queues And Pipes).

UNIT III SHARED MEMORY PROGRAMMING WITH OPENMP
Openmp Execution Model – Memory Model – Openmp Directives – Work-Sharing Constructs – Library Functions – Handling Data And Functional Parallelism – Handling Loops - Performance Considerations

UNIT IV DISTRIBUTED MEMORY PROGRAMMING WITH MPI

UNIT V PARALLEL PROGRAM DEVELOPMENT
Case Studies - N-Body Solvers – Tree Search – Openmp and MPI Implementations and Comparison

TOTAL:45 PERIODS
COURSE OUTCOMES:
At the end of the course, the student should be able to:
CO1: Illustrate the challenges in parallel and multi threaded programming
CO2: Explain the various parallel programming paradigms and solutions.
CO3: Develop shared memory programs using openmp
CO4: Develop distributed memory programs using mpi
CO5: Compare and contrast programming for serial processors and parallel processors.

REFERENCES

VE4005 RECONFIGURABLE COMPUTING

COURSE OBJECTIVES:
- To understand the need for reconfigurable computing
- To expose the students to various device architectures
- To examine the various reconfigurable computing systems
- To expose the students to HDL programming and familiarize with the development environment
- To develop applications with FPGAs

UNIT I DEVICE ARCHITECTURE 9

UNIT II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS 9

UNIT III PROGRAMMING RECONFIGURABLE SYSTEMS 9

UNIT IV MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS 9

UNIT V APPLICATION DEVELOPMENT WITH FPGAS 9
COURSE OUTCOMES:
Upon completion of the course, the students will be able to
CO1: Identify the need for reconfigurable architectures
CO2: Discuss the architecture of FPGAs
CO3: Point out the salient features of different reconfigurable architectures
CO4: Build basic modules using any HDL
CO5: Develop applications using any HDL and appropriate tools
CO6: Design and build an SOPC for a particular application

REFERENCES

VE4071 HARDWARE SOFTWARE CO-DESIGN

COURSE OBJECTIVES:
- To acquire the knowledge about system specification and modelling
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation

UNIT I SYSTEM SPECIFICATION AND MODELLING

UNIT II HARDWARE/SOFTWARE PARTITIONING
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis Hardware software synthesis algorithms: hardware – software partitioning, distributed system co-synthesis.
UNIT IV PROTOTYPING AND EMULATION

UNIT V DESIGN SPECIFICATION AND VERIFICATION

TOTAL: 45 PERIODS

COURSE OUTCOMES:
At the end of this course, the students should will be able to:
CO1: describe the broad range of system architectures and design methodologies that currently exist and define their fundamental attributes.
CO2: discuss the dataflow models as a state-of-the-art methodology to solve co-design problems and to optimize the balance between software and hardware.
CO3: understand in translating between software and hardware descriptions through co-design methodologies.
CO4: understand the state-of-the-art practices in developing co-design solutions to problems using modern hardware/software tools for building prototypes.
CO5: understand the concurrent specification from an algorithm, analyze its behavior and partition the specification into software (C code) and hardware (HDL) components.

REFERENCES

II4092 SYSTEM ON CHIP L T P C 3 0 0 3

COURSE OBJECTIVE:
- To introduce architecture and design concepts underlying system on chips.
- Students can gain knowledge of designing SoCs.
- To impart knowledge about the hardware-software design of a modest complexity chip all the way from specifications, modeling, synthesis and physical design.

UNIT I SYSTEM ARCHITECTURE: OVERVIEW
Components of the system – Processor architectures – Memory and addressing – system level interconnection – SoC design requirements and specifications – design integration – design
complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.

UNIT II PROCESSOR SELECTION FOR SOC 9

UNIT III MEMORY DESIGN 9

UNIT IV INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION 9

UNIT V FPGA BASED EMBEDDED PROCESSOR 9

TOTAL:45 PERIODS

COURSE OUTCOMES:
Upon successful completion of the program the students shall
- Explain all important components of a System-on-Chip and an embedded system, i.e.
- digital hardware and embedded software;
- Outline the major design flows for digital hardware and embedded software;
- Discuss the major architectures and trade-offs concerning performance, cost and power consumption of single chip and embedded systems;

REFERENCES:
COURSE OBJECTIVES:
- to introduce the concepts of Micro Electro Mechanical devices.
- to know the fabrication process of microsystems.
- to know the design concepts of micro sensors and micro actuators.
- to familiarize concepts of Quantum Mechanics and Nano systems.

UNIT I  OVERVIEW
New trends in Engineering and Science: Micro and Nanoscale systems, introduction to design of MEMS and NEMS, MEMS and NEMS – applications, devices and structures. Materials for MEMS: Silicon, Silicon compounds, polymers, metals

UNIT II  MEMS FABRICATION TECHNOLOGIES

UNIT III  MICRO SENSORS

UNIT IV  MICRO ACTUATORS

UNIT V  NANOSYSTEMS AND QUANTUM MECHANICS
Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave Function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their Quantization, Molecular Wires and Molecular Circuits

COURSE OUTCOMES:
At the end of this course, the student will be able to:
CO1:Discuss micro sensors
CO2:Explain micro actuators
CO3:Outline nanosystems and Quantum mechanics
CO4:Design micro actuators for different applications
CO5:Analyze atomic structures

REFERENCES

AP4091 AUTOMOTIVE ELECTRONICS L T P C 3 0 0 3

COURSE OBJECTIVES:
- To explain the principle of electronic management system and different sensors used in the systems.
- To know the concepts and develop basic skills necessary to diagnose automotive electronic problems.
- To know Starting, and charging, lighting systems, advanced automotive electrical systems.
- To include electronic accessories and basic computer control.
- To explore practically about the components present in an Automotive electrical and electronics system.

UNIT I FUNDAMENTALS 9
Components for electronic engine management system, open and closed loop control strategies, PID control, Look up tables, introduction to modern control strategies like Fuzzy logic and adaptive control. Switches, active resistors, Transistors, Current mirrors/amplifiers, Voltage and current references, Comparator, Multiplier. Amplifier, filters, A/D and D/A converters.

UNIT II MODERN SENSORS 9
Film sensors, micro-scale sensors, Particle measuring systems, Vibration Sensors, SMART sensors, Machine Vision, Multi-sensor systems Applications of Sensors: Applications and case studies of Sensors in Automobile Engineering, Aeronautics, Machine tools and Manufacturing processes.

UNIT III CHARGING SYSTEM 9

UNIT IV AUTOMOTIVE TRANSMISSION CONTROL SYSTEMS 9

UNIT V ELECTRONICS SYSTEMS 9
SUGGESTED ACTIVITIES:

1. Testing of battery, starting systems, charging systems, ignition systems and body controller systems
2. Study of various sensors and actuators used in two wheelers and four wheelers for electronic control.

COURSE OUTCOMES:
At the end of this course the students will be able to:

CO1: Explain the fundamentals, operation, function of various sensors and actuators in engine management systems.
CO2: Explain the Automotive Transmission Control Systems.
CO3: Enumerate the principles, application, construction and specification of different sensors and actuators usable in typical automobile by suitable testing.
CO4: List out the principles and characteristics of charging system components and demonstrate their working with suitable tools.
CO5: Describe the principles and architecture of electronics systems and its components present in an automobile related to instrumentation, control, security and warning systems.

TOTAL: 45 PERIODS

REFERENCES


VE4006 EMBEDDED WIRELESS SENSOR NETWORKS

COURSE OBJECTIVES:

- To discuss the overview of wireless sensor networks
- To familiarize the architecture of different networks
- To get knowledge about various physical layer and MAC protocols
- To acquire knowledge about different types of smart sensors used for designing the embedded system
- To know about the implementation of protocols on WSN in various applications
UNIT I  OVERVIEW OF WIRELESS SENSOR NETWORKS  9

UNIT II  NETWORK ARCHITECTURE  9
Single node architecture.-Hardware components-Energy consumption of sensor nodes- Operating systems and execution environments- Some examples of sensor nodes-Sensor Network Scenarios – Optimization Goals and Figure of Merit – Design Principles for WSNs – Gateway Concepts.

UNIT III  PHYSICAL LAYER AND MAC PROTOCOLS  9

UNIT IV  SMART SENSORS  9

UNIT V  APPLICATIONS AND PROTOCOL IMPLEMENTATION ON WSN  9

TOTAL:45 PERIODS

COURSE OUTCOMES:
At the end of this course, the students should will be able to:
CO1: Explain the basics of wireless sensor networks.
CO2: Discuss about the sensor network components, architecture and design principles of WSN
CO3: Explain the need of physical layer design challenges and MAC protocols.
CO4: Design the smart sensors and applications of WSN.
CO5: Improved employability and entrepreneurship capacity due to knowledge upgradation on recent trends in embedded systems design.

REFERENCES
COURSE OBJECTIVES:
- To give an introduction to and developing deeply embedded systems
- To familiarize the architecture and protocols in WSN
- To briefly study the application areas of network embedded systems

UNIT I  NETWORK EMBEDDED SYSTEMS: AN INTRODUCTION  9

UNIT II  WIRELESS SENSOR NETWORKS  9
Introduction To WSNS- Architecture for WSNS- Localization & Synchronization for WSN- Time Sync Issues & Resource Aware Localization

UNIT III  POWER AND ENERGY IN WSN  9

UNIT IV  AUTOMOTIVE NETWORKED EMBEDDED SYSTEMS  9
Time – Triggered Communication- Networks In Automotive Systems - Controller Area Networks, Flex Ray Communications, Lin Self-Study Automotive Examples Volcano

UNIT V  INDUSTRIAL AUTOMATION  9

COURSE OUTCOMES:
At the end of this course, the students should will be able to:
CO1: understand the basics of network systems
CO2: discuss about the sensor network components, architecture and design principles of WSN
CO3: Explain the need MAC protocols and energy conservation
CO4: application of networked automotive system
CO5: design and development of home automation

REFERENCES
2. G.Pottie, W.Kaiser, Principles of Embedded Networked System Design
COURSE OBJECTIVES:
- to study the various impedance matching techniques used in RF circuit design.
- to understand the functional design aspects of LNAs, Mixers, PLLs and VCOs.
- to understand frequency synthesis.

UNIT I  IMPEDANCE MATCHING IN AMPLIFIERS  9

UNIT II  AMPLIFIER DESIGN  9
Noise Characteristics of MOS Devices, Design of CG LNA and Inductor Degenerated LNAs. Principles of RF Power Amplifiers Design

UNIT III  ACTIVE AND PASSIVE MIXERS  9

UNIT IV  OSCILLATORS  9
LC Oscillators, Voltage Controlled Oscillators, Ring Oscillators, Delay Cells, Tuning Range in Ring Oscillators, Tuning in LC Oscillators, Tuning Sensitivity, Phase Noise in Oscillators, Sources of Phase Noise

UNIT V  PLL AND FREQUENCY SYNTHESIZERS  9
Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase Noise in PLL, Loop Bandwidth, Basic Integer-N Frequency Synthesizer, Basic Fractional-N Frequency Synthesizer

TOTAL:45 PERIODS

COURSE OUTCOMES:
At the end of this course, the students will be able to:

CO1: to understand the principles of operation of an RF receiver front end
CO2: to design and apply constraints for LNAs, Mixers and frequency synthesizers
CO3: to analyze and design mixers
CO4: to design different types of oscillators and perform noise analysis
CO5: to design PLL and frequency synthesizer

REFERENCES
COURSE OBJECTIVES:
- Understand static and dynamic characteristics of measurement systems.
- Study various types of sensors.
- Study different types of actuators and their usage.
- Study State-of-the-art digital and semiconductor sensors.

UNIT I  INTRODUCTION TO MEASUREMENT SYSTEMS  9
Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance characteristics: static and dynamic characteristics of measurement systems, zero-order, first-order, and second-order measurement systems and response.

UNIT II  RESISTIVE AND REACTIVE SENSORS  9
Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & application to LVDT.

UNIT III  SELF-GENERATING SENSORS  9

UNIT IV  ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS  9
Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.

UNIT V  DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS  9
Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, MOSFET transistors, CCD imaging sensors, ultrasonic sensors, fiber-optic sensors.

COURSE OUTCOMES:
Upon completion of the course the student will be able to:
CO1: Compare Actuators with various drive characteristics.
CO2: Evaluate digital sensors and semiconductor device sensors performance metrics.
CO3: Characterize the performance of Self-generating sensors.

TOTAL: 45 PERIODS
CO4: Analyze the performance of self-generating Sensors.
CO5: Analyze the performance of resistive and reactive sensors.

REFERENCES:

VE4008 REAL TIME OPERATING SYSTEMS

COURSE OBJECTIVES:
- To learn about significance and usage of Real Time Operating System
- To learn about different scheduling strategies and optimization principles
- To learn about the resource allocation or sharing process involved in RTOS
- To study about the different firmware and tools related to RTOS development
- To design and develop an innovative real time embedded system

UNIT I REAL TIME EMBEDDED SYSTEMS

UNIT II RESOURCES AND SERVICES
Processing - Resources - Memory - Multiresource Services : Blocking, Deadlock, Livelock, Critical Sections To Protect Shared Resources, Priority Inversion, Power Management And Processor Clock Modulation - Soft Real Time Services : Missed Deadlines, Quality of Service, Alternatives To Rate Monotonic Policy, Mixed Hard and Soft Real Time Services

UNIT III REAL TIME EMBEDDED COMPONENTS
Hardware Components - Firmware Components - RTOS System Software - Software Application Components - Traditional Hard Real Time Operating Systems : Asymmetric Multicore Processing And Symmetric Multi-Core Processing - Processor Core Affinity - SMP Support Models - RTOS Hypervisors - Open Source Real Time Operating Systems
UNIT IV  INTEGRATING EMBEDDED LINUX

Integrating Embedded Linux Into Real Time Systems - Debugging Components - Performance Tuning - High Availability And Reliability Design - Hierarchical Approaches for Fail-Safe Design.

UNIT V  CASE STUDIES

System Life Cycle - Continuous Media Applications - Video and Audio Processing - Robotic Applications - Computer Vision Applications

TOTAL: 45 PERIODS

PRACTICAL EXERCISES:

Laboratory Exercises On Task Scheduling
1. Implement a Linux process that is executed at the default priority for a user-level application and waits on a binary semaphore to be given by another application. Run this process and verify its state using the ps command to list its process descriptor. Now, run a separate process to give the semaphore causing the first process to continue execution and exit. Verify completion.
2. Create An Application That Creates Two Tasks That Wait On a Timer Whilst the Main Task Loops.
3. Develop an Applications Using Linux
4. Design of Plant Control System

TOTAL: 30 PERIODS

COURSE OUTCOMES:
On successful completion of this course, students will be able to

CO1: complete understanding of scheduling algorithm and process
CO2: better understanding on firmware and tools related to the development of RTOS
CO3: to be able to design and develop an embedded system with RTOS functionality
CO4: to be able to design and develop the systems in Linux environments
CO5: to be able to develop large real-time embedded systems

REFERENCES:
VE4009  EMBEDDED NETWORKING  L T P C  3 0 2 4

COURSE OBJECTIVES:

- To learn the concepts of serial and parallel communication protocols
- To understand the application development using USB and CAN bus for PIC microcontrollers
- To learn the basics of ethernet
- To learn the application development using embedded internet
- To learn the wireless sensor network communication protocols

UNIT – I  COMMUNICATION PROTOCOLS  9

UNIT – II  USB AND CAN BUS  9

UNIT – III  ETHERNET BASICS  9

UNIT – IV  EMBEDDED ETHERNET  9

UNIT – V  EMBEDDED WIRELESS SENSOR NETWORKS  9

TOTAL: 45 PERIODS

PRACTICAL EXERCISES:  30 PERIODS
1. Write a Simple Application Program USB and PIC Interface.
2. Write a Simple Application Program Using CAN And PCI.
3. Write a Program for Email Transferring Using UDP And TCP
4. Write a Program for Energy Harvesting In WSN Node
5. Develop An Application Using Embedded Wireless Sensor Networks

TOTAL:45+30=75 PERIODS

COURSE OUTCOMES:
On successful completion of this course, students will be able to
CO1: analyze the wired and wireless network protocols
CO2: Design an application using embedded networking
CO3: Analyze the basics of Ethernet
CO4: Incorporate networks in embedded systems
CO5: Analyze the basics of wireless sensor networks

REFERENCES:

IF4071 DEEP LEARNING L T P C 3 0 2 4

COURSE OBJECTIVES:
- Develop and Train Deep Neural Networks.
- Develop a CNN, R-CNN, Fast R-CNN, Faster-R-CNN, Mask-RCNN for detection and recognition
- Build and train RNNs, work with NLP and Word Embeddings
- The internal structure of LSTM and GRU and the differences between them
- The Auto Encoders for Image Processing

UNIT I DEEP LEARNING CONCEPTS 6

UNIT II NEURAL NETWORKS 9

UNIT III CONVOLUTIONAL NEURAL NETWORK 10
UNIT VI  NATURAL LANGUAGE PROCESSING USING RNN  10

UNIT V  DEEP REINFORCEMENT & UNSUPERVISED LEARNING  10

SUGGESTED ACTIVITIES : (Experiments in Lab)  30
1: Feature Selection from Video and Image Data
2: Image and video recognition
3: Image Colorization
4: Aspect Oriented Topic Detection & Sentiment Analysis
5: Object Detection using Autoencoder

COURSE OUTCOMES:
CO1: Feature Extraction from Image and Video Data
CO2: Implement Image Segmentation and Instance Segmentation in Images
CO3: Implement image recognition and image classification using a pretrained network (Transfer Learning)
CO4: Traffic Information analysis using Twitter Data
CO5: Autoencoder for Classification & Feature Extraction

REFERENCES
1. Deep Learning A Practitioner’s Approach Josh Patterson and Adam Gibson O'Reilly Media, Inc.2017
2. Learn Keras for Deep Neural Networks, Jojo Moolayil, Apress,2018
4. Deep Learning with Python, FRANÇOIS CHOLLET, MANNING SHELTER ISLAND,2017

TOTAL: 45+30=75 PERIODS
COURSE OBJECTIVES:
- To understand the basics of embedded system and ARM architecture
- To understand the RTOS concepts like scheduling and memory management related to the embedded system
- To learn about the programming aspects of RTOS
- To learn the different protocols of embedded wireless application
- To understand concepts involved in the design of hardware and software components for an embedded system

UNIT I INTRODUCTION

UNIT II EMBEDDED/REAL TIME OPERATING SYSTEM

UNIT III CONNECTIVITY

UNIT IV REAL TIME UML

UNIT V SOFTWARE DEVELOPMENT AND APPLICATION

TOTAL: 45 PERIODS
PRACTICAL EXERCISES: 30 PERIODS
1. Read Input From Switch And Automatic Control/Flash LED for ARM Processor
2. Laboratory Exercises On Task Scheduling
3. Simple Program In Linux, Rtlinux And Vxworks
4. Develop a Real Time Security Monitoring System
COURSE OUTCOMES:
On successful completion of this course, students will be able to
CO1: Make a choice of suitable embedded processor for a given application
CO2: Design the hardware and software for the embedded system
CO3: Design and develop the real time kernel/operating system functions, task control block
structure and analyze different task states
CO4: Implement different types of inter task communication and synchronization techniques
CO5: Know about the aspects embedded connectivity in real time systems

TOTAL:45+30=75 PERIODS

REFERENCES:
4. B.P.Douglass, “Real Time Uml - Advances In the UML for Real-Time Systems, 3rd
7. Wayne Wolf, “Computers As Components - Principles of Embedded Computer System
Design”, Mergen Kaufmann Publisher, 2006.

VE4010 PERSUASIVE COMPUTING

OBJECTIVES:
- To understand the characteristics and principles of pervasive computing and the solutions
  that are in use
- To realize the role of wireless protocols in shaping the future internet
- To design and implement pervasive applications
- To introduce the enabling technologies of pervasive computing

UNIT I PERSUASIVE COMPUTING CONCEPTS
Perspectives of Pervasive Computing, Challenges, Technology; the Structure and Elements of
Pervasive Computing Systems: Infrastructure and Devices, Middleware for Pervasive Computing
Systems, Pervasive Computing Environments

UNIT II CONTEXT COLLECTION, USER TRACKING, AND CONTEXT
REASONING
Environments, Transparent Task Migration, Implementation and Illustrations.

UNIT III HCI INTERFACE IN PERSUASIVE ENVIRONMENT
HCI Service and Interaction Migration, Context- Driven HCI Service Selection, Scenario Study:
Video Calls At a Smart Office, a Web Service– Based HCI Migration Framework.
UNIT IV  PERVERSIVE MOBILE TRANSACTIONS  9
Mobile Transaction Framework, Context-Aware Pervasive Transaction Model, Dynamic
Transaction Management, Formal Transaction Verification, Evaluations

UNIT V  CASE STUDIES  9
ICAMPUS Prototype, IPSPACE: AN IPV6-Enabled Intelligent Space

TOTAL:45 PERIODS

PRACTICAL EXERCISES:  30 PERIODS
1. To Design the Software for Mobile Phones Using Symbion Os
   i. Text String Handling
   ii. Graphical Application
   iii. Dialog Application
   iv. Drawing Application
   v. File Handling Operations
3. Case Studies- Projects In Pervasive Computing- To Explore Wearable And Handheld Computing And Their Enabling Technologies

COURSE OUTCOMES:
At the end of this course, the students should will be able to:
CO1: Outline the basic problems, performance requirements of pervasive computing applications,
    and the trends of pervasive computing and its impacts on future computing applications and society
CO2: Analyze and compare the performance of different data dissemination techniques and
    algorithms for mobile real-time applications
CO3: Analyze the performance of different sensor data management and routing algorithms for
    sensor networks
CO4: Develop an attitude to propose solutions with comparisons for problems related to pervasive
    computing system through investigation
CO5: Study on application on IPv6.

TOTAL:45+30=75 PERIODS

REFERENCES
COURSE OBJECTIVES:

- Understand the concepts of physical design process such as partitioning, floorplanning, placement and routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI design automation.
- Formulate CAD design problems using algorithmic methods.

UNIT I  INTRODUCTION  

UNIT II  FLOOR-PLANNING:
Planning: Hierarchical Design, Wire Length Estimation, Slicing and Non-Slicing Floor Plan, Polar Graph Representation, Operator Concept, Stockmeyer Algorithm for Floor Planning, Mixed Integer Linear Program.

UNIT III  PLACEMENT
Design Types: ASICs, SOC, Microprocessor RLM; Placement Techniques: Simulated Annealing, Partition Based, Analytical, and Hall’s Quadratic; Timing and Congestion Considerations.

UNIT IV  ROUTING
Detailed, Global and Specialized Routing, Channel Ordering, Channel Routing Problems and Constraint Graphs, Routing Algorithms, Yoshimura And Kuh’s Method, Zone Scanning and Net Merging, Boundary Terminal Problem, Minimum Density Spanning Forest Problem, Topological Routing, Cluster Graph Representation.

UNIT V  SEQUENTIAL LOGIC OPTIMIZATION AND CELL BINDING
State Based Optimization, State Minimization, Algorithms; Library Binding and Its Algorithms, Concurrent Binding.

TOTAL: 45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1. Graph Algorithms
   - Graph Search Algorithms
   - Spanning Tree Algorithm
   - Shortest Path Algorithm
   - Steiner Tree Algorithm

2. Partitioning Algorithms
   - Group Migration Algorithms
   - Simulated Annealing And Evolution Algorithms
   - Metric Allocation Method
3. Floor Planning Algorithms
   - Constraint Based Methods
   - Integer Programming Based Method
   - Rectangular Dualization Based Methods
   - Hierarchical Tree Based Methods
   - Simulated Evolution Algorithms
   - Time Driven Floor planning Algorithms

4. Routing Algorithms
   - Two Terminal Algorithms
   - Multi Terminal Algorithm

COURSE OUTCOMES:
At the end of this course, the students should will be able to:
CO1: Students can know how to place the blocks and how to partition the blocks while for designing the layout for IC.
CO2: Students can solve the performance issues in circuit layout.
CO3: Students are able to analyze physical design problems and employ appropriate automation algorithms for partitioning, floor planning, placement and routing.
CO4: Students can decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing.
CO5: Students can analyze circuits using both analytical and CAD tools

TOTAL: 45+30=75 PERIODS

REFERENCES

AUDIT COURSES

AX4091 ENGLISH FOR RESEARCH PAPER WRITING L T P C
2 0 0 0

COURSE OBJECTIVES

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission
UNIT I INTRODUCTION TO RESEARCH PAPER WRITING  6
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II PRESENTATION SKILLS  6

UNIT III TITLE WRITING SKILLS  6
Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV RESULT WRITING SKILLS  6
Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V VERIFICATION SKILLS  6
Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first-time submission

TOTAL: 30 PERIODS

COURSE OUTCOMES
CO1 – Understand that how to improve your writing skills and level of readability
CO2 – Learn about what to write in each section
CO3 – Understand the skills needed when writing a Title
CO4 – Understand the skills needed when writing the Conclusion
CO5 – Ensure the good quality of paper at very first-time submission

REFERENCES:

AX 4092 DISASTER MANAGEMENT  L T P C
2 0 0 0

COURSE OBJECTIVES
• Summarize basics of disaster
• Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
• Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
• Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
• Develop the strengths and weaknesses of disaster management approaches
UNIT I  INTRODUCTION  6
Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II  REPERCUSSIONS OF DISASTERS AND HAZARDS  6

UNIT III  DISASTER PRONE AREAS IN INDIA  6
Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT IV  DISASTER PREPAREDNESS AND MANAGEMENT  6
Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V  RISK ASSESSMENT  6
Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People’s Participation in Risk Assessment. Strategies for Survival

TOTAL : 30 PERIODS

COURSE OUTCOMES:
CO1: Ability to summarize basics of disaster
CO2: Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
CO3: Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
CO4: Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
CO5: Ability to develop the strengths and weaknesses of disaster management approaches

REFERENCES:

AX4093  CONSTITUTION OF INDIA  L T P C
2 0 0 0

COURSE OBJECTIVES:
Students will be able to:
• Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
• To address the growth of Indian opinion regarding modern Indian intellectuals’ constitutional role and entitlement to civil and economic rights as well as the emergence of Indian nationalism.
• To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

UNIT I  HISTORY OF MAKING OF THE INDIAN CONSTITUTION
History, Drafting Committee, (Composition & Working)

UNIT II  PHILOSOPHY OF THE INDIAN CONSTITUTION
Preamble, Salient Features

UNIT III  CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES

UNIT IV  ORGANS OF GOVERNANCE
Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V  LOCAL ADMINISTRATION

UNIT VI  ELECTION COMMISSION
Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS

COURSE OUTCOMES:
Students will be able to:
• Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
• Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
• Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
• Discuss the passage of the Hindu Code Bill of 1956.

SUGGESTED READING
1. The Constitution of India, 1950 (Bare Act), Government Publication.

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<tr>
<th>UNIT I</th>
<th>Tamil Literature</th>
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UNIT V

1. நவீன தமிழ் இலக்கியம்
   - குழுவினால் புத்தகங்கள்
   - குழுவினால் நம்பிகள்
   - குழுவினால் குறுக்குடேசம்
   - பார்வை இலக்கியம்
   - உடல்
2. நூற்றாண்டு விடுத்தகல் இலக்கியம்
3. சுற்றுச்சூழல் இலக்கியம்
4. பயண இலக்கியம் நூற்றாண்டு இலக்கியம்
5. கல்லுறுத்துப் பள்ளிக் கல்விக்கழகம்
6. கல்லுறுத்துப் பள்ளிக் கல்விக்கழகம்
7. அறிவியல் கல்லுறுத்துப் பள்ளிக் கல்விக்கழகம்

TOTAL: 30 PERIODS

தமிழ் விக்கிப்பீட்டு / புத்தகங்கள்

1. தமிழ் விக்கிப்பீட்டு (Tamil Virtual University)
   - www.tamilvu.org
2. தமிழ் விக்கிப்பீட்டு (Tamil Wikipedia)
   - https://ta.wikipedia.org
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