

ANNA UNIVERSITY, CHENNAI
NON- AUTONOMOUS COLLEGES
AFFILIATED TO ANNA UNIVERSITY
M.E., VLSI DESIGN
REGULATIONS 2025

PROGRAMME OUTCOMES (POs):

PO	Programme Outcomes
PO1	An ability to independently carry out research /investigation and development work to solve practical problems
PO2	An ability to write and present a substantial technical report/document.
PO3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

PROGRAMME SPECIFIC OUTCOMES(PSOs):

PSO	Programme Specific Outcomes
PSO1	Ability to design and implement innovative solutions to solve complex problems in VLSI.
PSO2	Competence to independently undertake research projects involving simulation, measurement, and product development in VLSI-related fields.



POST GRADUATE CURRICULUM (NON-AUTONOMOUS AFFILIATED INSTITUTIONS)

Programme: M.E., VLSI Design

Regulations: 2025

Abbreviations:

BS – Basic Science (Mathematics, Physics, Chemistry)

L – Laboratory Course

ES – Engineering Science (General (**G**), Programme Core (**PC**), Programme Elective (**PE**))

T – Theory

SD – Skill Development

LIT – Laboratory Integrated Theory

SL – Self Learning

PW – Project Work

TCP – Total Contact Period(s)

Semester I

S. No.	Course Code	Course Title	Type	Periods per week			Total Contact Periods	Credits	Category
				L	T	P			
1.	VL25101	Graph Theory and Optimization Techniques	T	3	1	0	4	4	ES (PC)
2.	VL25102	ASIC and FPGA Design	LIT	3	0	2	5	4	ES (PC)
3.	AP25C03	Digital CMOS VLSI Design	T	3	0	0	3	3	ES (PC)
4.	AP25C01	Advanced Digital System Design	T	3	1	0	4	4	ES (PC)
5.	AP25C02	Analog Integrated Circuit Design	T	3	0	0	3	3	ES (PC)
6.	AP25C04	Analog IC Design Laboratory	L	0	0	4	4	2	ES (PC)
7.	VL25103	Technical Seminar	-	0	0	2	2	1	SD
Total							25	21	

Semester II

S. No.	Course Code	Course Title	Type	Periods per week			Total Contact Periods	Credits	Category
				L	T	P			
1.	VL25201	Multi-Core Architecture and ISA Verification	T	3	0	0	3	3	ES (PC)
2.	VL25202	Data Converters IC Design	T	3	0	0	3	3	ES (PC)
3.	VL25203	VLSI testing and verification using UVM	T	3	0	0	3	3	ES (PC)
4.		Programme Elective I	T	3	0	0	3	3	ES (PC)
5.	VL25204	Low Power VLSI Design	T	3	0	0	3	3	ES (PC)
6.	-	Industry Oriented Course I	--	1	0	0	1	1	SD
7.	VL25205	Verification using UVM Laboratory	L	0	0	4	4	2	ES (PC)
8.	VL25206	Industrial Training	-	-	--	-	---	1	SD
9.	-	Self-Learning Course	-	-	--	-	---	1	--
Total							22	20	

Semester III

S. No.	Course Code	Course Title	Type	Periods per week			Total Contact Periods	Credits	Category
				L	T	P			
1.		Programme Elective II	T	3	0	0	3	3	ES (PE)
2.		Programme Elective III	T	3	0	0	3	3	ES (PE)
3.		Programme Elective IV	T	3	0	0	3	3	ES (PE)
4.	-	Programme Elective V	T	3	0	0	3	3	ES (PE)
	-	Industry Oriented Course I	--	1	0	0	1	1	SD
5.	VL25301	Project Work I	--	0	0	8	12	6	SD
Total							25	19	

Semester IV

S. No.	Course Code	Course Title	Type	Periods per week			Total Contact Periods	Credits	Category
				L	T	P			
1.	VL25401	Project Work II	--	0	0	24	24	12	
Total							24	12	

Programme Elective Courses (PE)

S. No.	Course Code	Course Title	Periods per week			Total Contact Periods	Credits
			L	T	P		
1.	VL25001	VLSI Signal Processing	3	0	0	3	3
2.	EL25C04	RF Integrated Circuit Design	3	0	0	3	3
3.	EL25C05	Electromagnetic Interference and Compatibility	3	0	0	3	3
4.	VL25002	Physical Design of VLSI	3	0	0	3	3
5.	AP25C06	Hardware / Software Co-Deign	3	0	0	3	3
6.	VL25003	CAD for VLSI Design	3	0	0	3	3
7.	VL25004	Nanotechnology	3	0	0	3	3
8.	VL25005	Pattern Recognition	3	0	0	3	3
9.	AP25C05	Signal Integrity for High Speed Design	3	0	0	3	3
10.	VL25006	Network On Chip	3	0	0	3	3
11.	VL25C01	VLSI for wireless Communication	3	0	0	3	3
12.	VL25007	DSP Structures for VLSI	3	0	0	3	3
13.	VL25C02	MEMS and NEMS	3	0	0	3	3
14.	VL25008	Advanced Transistor Modelling	3	0	0	3	3
15.	VL25009	VLSI Architectures for Image Processing	3	0	0	3	3
16.	VL25010	Reconfigurable Architecture	3	0	0	3	3
17.	VL25011	Adaptive Signal Processing	3	0	0	3	3
18.	VL25C03	Digital Image and Video Processing	3	0	0	3	3
19.	VL25012	Evolvable Hardware	3	0	0	3	3

Semester I

VL25101	Graph Theory and Optimization Techniques	L	T	P	C
		3	1	0	4
Course Objectives: <ul style="list-style-type: none"> Introduce and apply graph theory, linear and nonlinear programming, and simulation modeling techniques to solve real-life engineering and business problems. 					
Graphs: Graphs and graph models - Graph terminology and special types of graphs - Matrix representation of graphs and graph isomorphism - Connectivity- Euler and Hamilton paths - Trees - Spanning trees. Activities: 1. Construct and analyze graph models using adjacency matrices. 2. Identify Euler, Hamilton paths, and spanning trees in graphs.					
Graph Algorithm: Graph Algorithms - Directed graphs - Some basic algorithms - Shortest path algorithms - Depth - First search on a graph - Theoretic algorithms - Performance of graph theoretic algorithms - Graph theoretic computer languages. Activities: 1. Implement DFS and BFS on directed graphs. 2. Apply shortest path algorithms and analyze their performance.					
Linear Programming: Formulation - Graphical solution - Simplex method - Two-phase method - Transportation and Assignment Models. Activities: 1. Formulate and solve LP problems using graphical and simplex methods. 2. Solve transportation and assignment problems with two-phase method.					
Non-Linear Programming: Constrained Problems, Equality constraints- Lagrangean Method, Inequality constraints, Karush, Kuhn-Tucker {KKT} conditions - Quadratic Programming. Activities: 1. Solve constrained optimization using Lagrangean and KKT conditions. 2. Apply quadratic programming to nonlinear optimization problems.					
Simulation Model and Network Model: Monte Carlo Simulation, Types of Simulation, Elements of Discrete Event Simulation, Generation of Random Numbers, Applications to Queuing systems - Project network, CPM and PERT networks, Critical path scheduling - Sequencing models Activities: 1. Perform Monte Carlo and discrete event simulations for queuing systems. 2. Construct CPM/PERT networks and apply critical path scheduling.					
Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%					
Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).					

References:

1. Sharma, J. K. (2009). Operation Research (3rd ed.). Macmillan Publishers India Ltd.
2. West, D. B. (2015). Introduction to graph theory. Pearson Education.
3. Balakrishna, R., & Ranganathan, K. (2012). A textbook of graph theory. Springer Science and Business Media.
4. Deo, N. (2016). Graph theory with applications to engineering and computer science. Dover Publications, Inc.
5. Rao, G. S. S. B. (2015). Discrete structures and graph theory. Scitech Publications Pvt. Limited.
6. Natarajan, A. M., Balasubramani, P., & Tamilarasi, A. (2014). Operations research. Pearson Education Pvt. Limited.

	CO description	PO	PSO1	PSO2
CO1	Explain the basics of linear and nonlinear programming	-	-	-
CO2	Apply fundamental graph algorithms including shortest path and traversal techniques.	PO1(3) PO2(3)	3	3
CO3	Model and analyze graphs and their connectivity for problem-solving.	PO1(3) PO2(3)	2	2
CO4	Utilize simulation and network models like Monte Carlo, CPM, and PERT for engineering applications.	PO1(3) PO3(3)	3	2

VL25102	ASIC and FPGA Design	L	T	P	C
		3	0	2	4
<p>Course Objectives:</p> <p>To Focus on Semi-Custom IC Design: Principles of Logic Cells, I/O Cells, Interconnect Architecture; Equal emphasis on FPGA & ASIC styles.</p>					
<p>Introduction to Asics, CMOS Logic and ASIC Library Design: Types of Asics - Design Flow - CMOS Transistors - Combinational Logic Cell - Sequential Logic Cell - Data Path Logic Cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical Effort.</p> <p>Activity :Analyze and classify different types of ASICs based on their applications and design complexity.</p> <p>Practical Experiments:</p> <ol style="list-style-type: none"> 1. Simulate CMOS inverter circuits and study transistor parasitic effects using a circuit simulator tool. 2. Running simulator and debug tools 3. Experiment with 2 state and 4 state data types 					
<p>Programmable ASICS, Programmable ASIC Logic Cells and Programmable Asic I/O Cells: Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks, ASIC Tool Flow.</p> <p>Activity: Compare different programmable ASIC technologies (Anti-fuse vs SRAM vs EPROM) in terms of speed, power, and reconfigurability.</p> <p>Practical Experiments:</p> <ol style="list-style-type: none"> 1. Experiment with blocking and non-blocking assignments 2. Model and verify simple ALU 3. Model and verify an Instruction stack 					
<p>Logic Synthesis, Simulation and Testing: Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test-fault simulation - automatic test pattern generation.</p> <p>Activities:</p> <ol style="list-style-type: none"> 1: Write simple Verilog/VHDL modules and synthesize them using logic synthesis tools. 2: Perform functional and timing simulations and create testbenches for boundary scan testing. <p>Practical Experiments:</p> <ol style="list-style-type: none"> 1. Use an interface between testbench and DUT 2. Developing a test program 3. Create a simple and advanced OO testbench 					
<p>ASIC Physical Design: System partition -partitioning - partitioning methods - interconnect delay models and measurement of delay - floor planning - placement - Routing: global routing - detailed routing - special routing - circuit extraction – DRC</p>					

Activities:

- 1: Perform manual floor planning and placement for a simple ASIC design using CAD tools.
- 2: Analyze routing challenges and use tools to perform global and detailed routing; verify design rules compliance.

Practical Experiments:

1. Create a scoreboard using dynamic array
2. Use mailboxes for verification

FPGA: FPGA Building Block Architecture- Xilinx XC4000 - ALTERA's FLEX 8000/10000, ACTEL's ACT-1,2,3 FPGA Interconnect Routing Procedures.

Activities:

- 1: Explore and document the internal architecture of Xilinx XC4000 or Altera FLEX FPGA through data sheets.
- 2: Design and implement a simple combinational circuit on an FPGA development board and analyze routing.

Practical Experiments:

1. Generate constrained random test values
2. Using coverage with constrained random tests

Weightage: Continuous Assessment: 50%, End Semester Examinations: 50%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Smith, J. S. (2003). Application-specific integrated circuits. Pearson.
2. Smith, D. J. (1996). HDL chip design. Doone Publications.
3. Chan, K., & Mourad, S. (1994). Digital design using field programmable gate array. Prentice Hall.
4. Nekoogar, F. (1999). Timing verification of application-specific integrated circuits (ASICs). Prentice Hall PTR.
5. Wolf, W. (2004). FPGA-based system design. Prentice Hall PTR.
6. Kilts, S. (n.d.). Advanced FPGA design. Wiley Interscience.

	CO description	PO	PSO1	PSO2
CO1	Understand ASIC types, design flow, and CMOS logic fundamentals.	-	-	-
CO2	Design and analyze combinational and sequential logic cells in ASICs.	PO1(3) PO2(3)	3	3
CO3	Apply programmable ASIC technologies and use relevant design tools.	PO1(3) PO2(3)	2	2
CO4	Perform logic synthesis, simulation, physical design, and FPGA implementation.	PO1(3) PO3(3)	3	2

AP25C03	Digital CMOS VLSI Design	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <p>To Understand CMOS basics and design combinational/sequential circuits; apply structured VLSI design through case studies.</p>					
<p>MOS Transistors and CMOS Inverter: MOS transistor characteristics, short channel effects, CMOS inverter design, stick diagrams, power, delay, sizing. Activities: 1. Simulate CMOS inverter characteristics and sizing effects 2. Draw stick diagrams and analyze power-delay trade</p>					
<p>CMOS, Combinational Circuits: Complementary CMOS, power reduction, ratioed logic, pass transistor logic, dynamic CMOS, Domino, NP-CMOS. Activities: 1. Design combinational logic using different CMOS styles 2. Analyze power and switching activity in logic gates</p>					
<p>CMOS, Sequential Circuits: Latches vs registers, flip-flops, dynamic/static registers, clocking strategies, Schmitt trigger, mono/astable circuits. Activities: 1. Implement various flip-flops and compare timing behavior 2. Design clocking schemes for latch/register pipelines</p>					
<p>CMOS Sub System Design Adders (carry bypass, select, CLA), multipliers, counters, parity generators, multiplexers, shifters, memory elements. Activities: 1. Design fast adders and multipliers 2. Build and simulate small subsystems (e.g., counter + MUX)</p>					
<p>Performance Estimation & Design Techniques: Delay estimation, logical effort, sizing, power, interconnects, scaling, synchronous and self-timed design. Activities: 1. Estimate delay and power for sample circuits 2. Compare synchronous vs self-timed circuit design</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References</p> <ol style="list-style-type: none"> 1. Weste, N. H. E., & Harris, D. (2011). <i>CMOS VLSI design: A circuits and systems perspective</i>. Pearson. 2. Rabaey, J. M., & Nikolić, B. (2003). <i>Digital integrated circuits</i>. Pearson. 3. Martin, K. (2011). <i>Digital integrated circuit design</i>. Oxford University Press. 4. Palnitkar, S. (2003). <i>Verilog HDL</i> (2nd ed.). Pearson Education. 5. Rabaey, J. M., Chandrakasan, A., & Nikolić, B. (2003). <i>Digital integrated circuits</i>. Pearson. 					

	CO description	PO	PSO1	PSO2
CO1	Explain CMOS basics in digital circuits.	-	-	-
CO2	Analyze and design CMOS-based combinational and sequential circuits	PO1(3)	2	2
CO3	Apply various CMOS logic styles and techniques to optimize digital subsystems	PO1(3) PO2(3)	3	3
CO4	Evaluate and estimate circuit performance using structured approaches for subsystem design.	PO1(3) PO2(3)	2	2

AP25C01	Advanced Digital System Design	L	T	P	C
		3	1	0	4
<p>Course Objectives:</p> <p>To study design and analysis of synchronous/asynchronous sequential circuits, PLD/ROM design, combinational/PLA testing, and Verilog HDL for digital system design.</p>					
<p>Sequential Circuit Design: State diagrams/tables, state assignment & reduction, synchronous circuit design, iterative circuits, ASM charts.</p> <p>Activities: 1. Design state diagrams for given problems 2. Implement synchronous circuits using ASM</p>					
<p>Asynchronous Sequential Circuit Design: Flow table reduction, race conditions, hazards (static/dynamic/essential), mixed-mode circuits, vending machine controller design.</p> <p>Activities: 1. Analyze and minimize flow tables 2. Identify and eliminate hazards</p>					
<p>Fault Diagnosis and Testability Algorithms: Fault table, path sensitization, Boolean difference, D & Kohavi algorithms, PLA faults, DFT, BIST techniques.</p> <p>Activities: 1. Generate fault tables for combinational circuits 2. Simulate fault detection using D-algorithm</p>					
<p>Synchronous Design Using Programmable Devices: PLD families, PLA/PAL-based circuit design, ROM design, FSM realization using PLDs, FPGA (Xilinx Vertex 7).</p> <p>Activities: 1. Implement FSM using PLA/PAL 2. Program and simulate FSM on FPGA</p>					
<p>System Design Using Verilog: Verilog HDL modeling, data types, behavioral & structural modeling, FSM synthesis, test benches, combinational/sequential circuit realization.</p> <p>Activities: 1. Write and simulate Verilog code for registers, counters, serial adders 2. Design and test a simple microprocessor in Verilog</p>					
<p>Weightage: Continuous Assessment: 50%, End Semester Examinations: 50%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References:</p> <ol style="list-style-type: none"> Roth, C. H., Jr. (2013). Fundamentals of logic design (7th ed.). Thomson Learning. Arnold, M. G. (1999). Verilog digital – computer design. Prentice Hall PTR. Biswas, N. N. (2001). Logic design theory. Prentice Hall of India. Lala, P. K. (2020). Fault tolerant and fault testable hardware design. B S Publications. Lala, P. K. (2015). Digital system design using PLD (Reprint ed.). B S Publications. Palnitkar, S. (2003). Verilog HDL – A guide to digital design and synthesis. Pearson. 					

	CO description	PO	PSO1	PSO2
CO1	Explain the fundamentals of synchronous and asynchronous sequential circuits	-	-	-
CO2	Analyze and design sequential circuits using state diagrams and ASM charts.	PO1(3)	2	2
CO3	Apply fault diagnosis and testability algorithms to digital circuits.	PO1(3) PO2(3)	3	3
CO4	Develop and simulate digital systems using Verilog HDL and FPGA.	PO1(3) PO2(3)	2	2

AP25C02	Analog Integrated Circuit Design	L	T	P	C
		3	0	0	3
<p>Course Objectives: To Study single-stage amplifier design, high-frequency/noise characteristics, operational amplifiers, voltage/current reference circuits with practical exercises</p>					
<p>Single Stage Amplifiers: MOS physics, equivalent circuits, CS, CG, source follower, differential & cascode amplifiers, design for SR, gain, BW, ICMR, power, voltage swing. Activities: 1. Design and simulate CS, CG amplifiers 2. Calculate gain, bandwidth, slew rate for given specification</p>					
<p>High Frequency and Noise Characteristics of Amplifiers: Miller effect, pole analysis, frequency response of stages, noise sources, noise analysis in single stage and differential amplifiers. Activities: 1. Analyze frequency response using pole-zero plots 2. Simulate noise performance in amplifiers.</p>					
<p>Negative Feedback Amplifiers and Operational Amplifiers: Feedback types, loading effects, op-amp parameters, one/two-stage op-amps, gain boosting, slew rate, PSRR, noise in op-amps. Activities: 1. Design and simulate negative feedback circuits 2. Evaluate gain, slew rate, and PSRR of op-amps</p>					
<p>Stability and Frequency Compensation of Two Stage Operational Amplifier: Two-stage op-amp analysis, phase margin, compensation methods, slew rate issues, advanced compensation techniques. Activities: 1. Analyze phase margin and stability in two-stage op-amps 2. Implement frequency compensation methods in simulations</p>					
<p>Voltage and Current References: Current mirrors (Wilson, Widlar, Cascode), high swing cascode sinks, supply/temperature independent biasing, PTAT & CTAT currents, constant-Gm biasing. Activities: 1. Design and simulate various current mirrors 2. Implement PTAT and CTAT current references</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References:</p> <ol style="list-style-type: none"> Razavi, B. (2016). Design of analog CMOS integrated circuits (2nd ed.). Tata McGraw Hill. Sansen, W. M. C. (2007). Analog design essentials. Springer. Grebene, A. B. (2003). Bipolar and MOS analog integrated circuit design. John Wiley & Sons, Inc. Allen, P. E., & Holberg, D. R. (2013). CMOS analog circuit design (3rd ed.). Oxford University Press. Natarajan, A. (n.d.). EE5390: Analog IC Design [Recorded lecture]. Retrieved from http://www.ee.iitm.ac.in/~ani/ee5390/index.html 					

6. Baker, R. J. (2019). CMOS: Circuit design, layout, and simulation (4th ed.). Wiley IEEE Press.

	CO description	PO Mapping	PSO1	PSO2
CO1	Explain the theory and design concepts of analog circuits .	-	-	-
CO2	Analyse and design single-stage and multi-stage amplifiers considering high-frequency and noise characteristics to meet specified performance criteria.	PO1(3)	2	2
CO3	Apply concepts of negative feedback, stability, and frequency compensation in the design and analysis of operational amplifiers.	PO1(3) PO2(3)	3	3
CO4	Design and simulate voltage and current reference circuits with temperature and supply independence for analog integrated systems.	PO1(3) PO2(3)	2	2

AP25C04	Analog IC Design Laboratory	L	T	P	C
		0	0	4	2
<p>Course Objectives:</p> <p>To Design analog circuits from transistor level to IA implementation using CAD tools for simulation, layout, LVS, and parasitic extraction.</p>					
<p>List of Experiments</p> <ol style="list-style-type: none"> 1. Extraction of process parameters of CMOS process transistors <ol style="list-style-type: none"> a. Plot ID vs. VGS at different drain voltages for NMOS, PMOS. b. Plot ID vs. VGS at particular drain voltage for NMOS, PMOS and determine Vt. c. Plot log ID vs. VGS at particular gate voltage for NMOS, PMOS and determine IOFF and sub- threshold slope. d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor. e. Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS of appropriate voltage To extract Vth use the following procedure. <ol style="list-style-type: none"> i. Plot gm vs VGS using SPICE and obtain peak gm point. ii. Plot $y=ID/(gm)$ as a function of VGS using SPICE. iii. Use SPICE to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth. f. Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it. 2. CMOS inverter design and performance analysis <ol style="list-style-type: none"> a. i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter. ii. Plot VTC for CMOS inverter with varying VDD. iii. Plot VTC for CMOS inverter with varying device ratio. b. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay tpHL, tpLH, 20%-to-80% rise time tr and 80%-to-20% fall time tf. c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. 3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum. 4. Single stage amplifier design and performance analysis <ol style="list-style-type: none"> a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors. b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load. <ol style="list-style-type: none"> i. Establish a test bench to achieve $VDSQ=VDD/2$. ii. Calculate input bias voltage for a given bias current. 					

- iii. Use spice and obtain the bias current. Compare with the theoretical value
 - iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier
 - v. using small signal analysis in spice, considering load capacitance.
 - vi. Plot step response of the amplifier with a specific input pulse amplitude.
 - vii. Derive time constant of the output and compare it with the time constant
 - viii. resulted from -3dB Band Width.
 - ix. Use spice to determine input voltage range of the amplifier
5. Three OPAMP Instrumentation Amplifier (INA).
Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
- i. Draw the schematic of op-amp macro model.
 - ii. Draw the schematic of INA.
 - iii. Obtain parameters of the op-amp macro model such that it meets a given specification for: i.low-frequency voltage gain, ii. unity gain BW (f_u), iii.input capacitance, iv.output resistance, v.CMRR
- a. Draw schematic diagram of CMRR simulation setup.
 - b. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
 - c. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
 - d. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.
- 6.Use Layout editor.
- a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal 1 as interconnect line between inverters.
 - b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.
 - c. Extract the netlist. Use extracted netlist and obtain tPHL tPLH for the inverter using Spice.
 - d. Use a specific interconnect length and connect and connect three inverters in a chain.
 - e. Extract the new netlist and obtain tPHL and tPLH of the middle inverter.
 - f. Compare new values of delay times with corresponding values obtained in part 'c'.
7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter
- a. low-frequency voltage gain,
 - b. unity gain BW (f_u),
 - c. Power dissipation
 - i. Perform DC analysis and determine input common mode range and compare with the theoretical values.
 - ii. Perform time domain simulation and verify low frequency gain.
 - iii. Perform AC analysis and verify.

Weightage: Continuous Assessment: 60%, End Semester Examinations: 40%

Assessment Methodology: Project (30%), Assignment (10%), Practical (30%), Internal Examinations (30%)

	CO description	PO	PSO1	PSO2
CO1	Characterize MOS transistors and design basic analog building blocks using simulation tools.	PO1(3)	2	2
CO2	Implement and simulate analog circuits through schematic entry, layout design, LVS, and parasitic extraction.	PO1(3) PO2(3)	3	3
CO3	Design and validate an instrumentation amplifier using a structured analog design flow with CAD tools.	PO1(3) PO2(3)	2	2

Semester II

Introduction to Computer Organisation: Computer types – Functional units of a computer – Bus structures – Software – Processor clock – Performance equation – Pipelining and parallel processing – Compiler – Performance measurement – Multiprocessor and Multicomputer

Processor: CPU core architecture – Logic design conventions – Datapath – Pipelining Datapath and control – Data and control hazards – Exceptions – Single core to Multi-core architectures – SIMD and MIMD systems - ARM cortex A53 and Intel core i7 pipelines – Qualcomm Snapdragon 888 SoC

Instruction Set Architecture: RISC-V Instructions – Base, Single and Double precision floating point, Atomic, Compute instructions – Instruction set representation, Parallel Program Design

Memory Organisation: Memory hierarchy – Types of Memory – SRAM, DRAM, Flash memory, Disk – Cache memory – Cache hit and miss – Cache mapping – Direct mapping, Associative mapping and Set-associative mapping – DDR4 RAM

ISA Verification: Decimal to floating point converter design, Floating point arithmetic modules design and verification, OP-Code generation for integer, floating point, atomic, compressed instructions set.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. David Patterson and John. L. Hennessy – Computer Organization and Design (The hardware/software interface RISC-V Edition) Elsevier, 2018.
2. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”,. Tata McGraw Hill, Fifth Edition, 2002
3. Peter S. Pacheco, —An Introduction to Parallel Programming, Morgan-Kauffman/Elsevier, 2011
4. Andrew Waterman, Yunsup Lee, David Patterson, Krste Asanović, “The RISC-V Instruction Set Manual, Volume I: User-Level ISA Version 2.1”, Technical Report UCB/EECS-2016-118, EECS Department, University of California, Berkeley, May 31, 2016
5. Andrew Waterman, Yunsup Lee, Rimantas Avižienis, David A. Patterson, and Krste Asanović, “The RISC-V Instruction Set Manual, Volume II: Privileged Architecture Version 1.9”, Technical Report UCB/EECS-2016-129, EECS Department, University of California, Berkeley, July 8, 2016

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Explain computer organization, functional units, pipelining, parallel processing, and performance measurement of multi-core systems	-	-	-
CO2	Analyze CPU core architectures, pipeline design, hazards, exceptions, and SIMD/MIMD multi-core systems (ARM Cortex-A53, Intel i7, Snapdragon 888)	PO2(3), PO3(3), PO5(2)	3	2
CO3	Apply instruction set architecture (RISC-V) concepts including base, floating-point, atomic, and compute instructions for parallel program design	PO3(3), PO4(3), PO5(3)	3	3
CO4	Design and verify ISA modules including decimal-to-floating point converters, floating-point arithmetic modules, and opcode generation for integer, floating point, atomic, and compressed instructions	PO3(3), PO4(3), PO6(3), PO12(3)	3	3

Introduction & Characteristics of AD/DA Converter Characteristics: Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and antialiasing filters.

Switch Capacitor Circuits and Comparators: Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques

Nyquist Rate D/A Converters: Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues in current element matching, clock feed through, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs

Pipeline And Other ADCs: Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

Sigma Delta Converters: STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Opamp nonlinearities

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Shanthi Pavan, Richard Schreier, Gabor C. Temes , “Understanding Delta-Sigma Data Converters”, Willey –IEEE Press, 2nd Edition, 2017.
2. Behzad Razavi, “Principles of data conversion system design”, IEEE press, 1995.
3. M. Pelgrom, “Analog-to-Digital Conversion”, Springer, 4th Edition, January 2002.
4. Rudy van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters” Kluwer Academic Publishers, Boston, 2nd Edition, December 2010.
5. J. G. Proakis, D. G. Manolakis, “Digital Signal Processing Principles, Algorithms and Applications”, Prentice Hall, 4th Edition, January 2014.
6. VLSI Data Conversion Circuits EE658 recorded lectures available at <http://www.ee.iitm.ac.in/~nagendra/videolecture>

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Explain the characteristics, types, and applications of ADCs and DACs, including sampling, quantization, reconstruction, oversampling, and anti-aliasing	-	-	-
CO2	Analyze switched-capacitor circuits and comparators, including offset cancellation and calibration techniques	PO2(3), PO3(3), PO5(2)	3	2
CO3	Apply Nyquist-rate DAC and ADC design concepts including current-steering DACs, binary vs thermometer DACs, DNL, INL, and zero-order hold circuits	PO3(3), PO4(3), PO5(3)	3	3
CO4	Design and evaluate pipeline, flash, successive-approximation, time-interleaved, and sigma-delta ADC architectures with performance metrics and modulator characteristics	PO3(3), PO4(3), PO6(3), PO12(3)	3	3

VL25203	VLSI Testing and Verification Using UVM	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ul style="list-style-type: none"> To introduce the VLSI testing. To introduce logic and fault simulation and testability measures. To study the test generation for combinational and sequential circuit. To provide the students complete understanding on UVM testing To become proficient at UVM verification. 					
<p>Introduction to VLSI Testing Introduction - VLSI Testing Process and Test Equipment- Challenges in VLSI Testing - Test Economics and Product Quality- Fault Modelling - Relationship among Fault Models.</p>					
<p>Logic & Fault Simulation & Testability Measures Simulation for Design Verification and Test Evaluation - Modelling Circuits for Simulation - Algorithms for True Value and Fault Simulation - Scoap Controllability and observability</p>					
<p>Test Generation for Combinational and Sequential Circuits Algorithms and Representations - Redundancy Identification - Combinational ATPG Algorithms - Sequential ATPG Algorithms - Simulation Based ATPG - Genetic Algorithm Based ATPG</p>					
<p>Introduction to UVM Overview- The Typical UVM Test bench Architecture- The UVM Class Library- Transaction-Level Modelling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation</p>					
<p>Developing Reusable Verification Components Modelling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage.</p>					
<p>Activities</p> <ul style="list-style-type: none"> Do microcontroller based design experiments. Create program -state models for different embedded applications. Design and develop embedded solutions for real world problems. 					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References:</p> <ol style="list-style-type: none"> Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test Principles and Architectures", Elsevier, 2017 Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2017. Niraj K. Jha and Sandeep Gupta, "Testing of Digital Systems", Cambridge University Press, 2017 					

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Explain VLSI testing concepts, fault modeling, test economics, and product quality in chip verification	-	-	-
CO2	Analyze logic and fault simulation techniques, controllability/observability measures, and testability of combinational and sequential circuits	PO2(3), PO3(3), PO5(2)	3	2
CO3	Apply ATPG (Automatic Test Pattern Generation) algorithms, including combinational, sequential, simulation-based, and GA-based test pattern generation	PO3(3), PO4(3), PO5(3)	3	3
CO4	Design and implement reusable UVM verification components using TLM, agents, drivers, sequencers, monitors, environments, and test scenarios	PO3(3), PO4(3), PO6(3), PO12(3)	3	3

VL25204	Low Power VLSI Design	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ol style="list-style-type: none"> 1. Know the low power low voltage VLSI design 2. Understand the impact of power on system performances. 3. Know about different Design approaches. 4. Identify suitable techniques to reduce power dissipation in combinational and sequential circuits. 5. Understand the design of low power memories 					
<p>Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation - Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects - Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.</p> <p>Low-Power Design Approaches: Low-Power Design through Voltage Scaling: VT CMOS circuits, MTCMOS circuits, Architectural Level Approach - Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.</p> <p>Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures - Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low Voltage Low-Power Design Techniques - Trends of Technology and Power Supply Voltage, Low Voltage Low-Power Logic Styles.</p> <p>Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.</p> <p>Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References:</p> <ol style="list-style-type: none"> 1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis and Design", TMH, 2011. 2. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering. 3. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System 					

Perspective", CRC Press

4. Anantha Chandrakasan, "Low Power CMOS Design", IEEE Press, /Wiley International, 1998.
5. Kaushik Roy, Sharat C. Prasad, "Low Power CMOS VLSI Circuit Design", John Wiley, & Sons, 2000.
6. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 2002.
7. Bellamour, M. I. Elamasri, "Low Power CMOS VLSI Circuit Design", A Kluwer Academic Press.
8. Siva G. Narendran, Anatha Chandrakasan, "Leakage in Nanometer CMOS Technologies", Springer, 2005.

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Explain the fundamentals of low-power VLSI design, sources of power dissipation, and short-channel effects	-	-	-
CO2	Analyze and apply low-power design approaches at circuit and architectural levels, including voltage scaling, VTCMOS/MTCMOS, and switched-capacitance minimization	PO2(3), PO3(3), PO5(2)	3	2
CO3	Design low-voltage low-power arithmetic circuits: adders and multipliers using Ripple Carry, Carry Look-Ahead, Carry Select, Braun, Baugh-Wooley, Booth, and Wallace Tree architectures	PO3(3), PO4(3), PO5(3)	3	3
CO4	Design and evaluate low-power memories: ROM, SRAM, and DRAM using low-power techniques, precharge/equalization circuits, and self-refresh mechanisms	PO3(3), PO4(3), PO6(3), PO12(3)	3	3

COURSE OBJECTIVES:

- to help the engineers to design the system with verilog and system Verilog
- Complete understanding of Verilog Hardware Description Language
- to practice for writing synthesizable RTL models that work correctly in both simulation and synthesis.

LIST OF EXPERIMENTS

1. Simulate a simple UVM testbench and DUT
2. Examining the UVM testbench
3. Design and simulate sequence items and sequence
4. Design and simulate a UVM driver and sequencer
5. Design and simulating UVM monitor and agent
6. Design, simulate and examine coverage
7. Design and simulate a UVM scoreboard and environment, and verifying the outputs of a (faulty) DUT
8. Design and simulate a test that runs multiple sequence
9. Design and simulate a configurable UVM test environment

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Apply Verilog and System Verilog for designing and simulating digital systems	PO1(3), PO2(3), PO3(2)	3	2
CO2	Develop and simulate UVM testbenches including sequence items, drivers, sequencers, monitors, and agents	PO2(3), PO3(3), PO4(2)	3	2
CO3	Implement verification components such as coverage, scoreboard, and configurable UVM environments	PO3(3), PO4(3), PO5(2)	3	3
CO4	Analyze and verify DUT functionality using UVM environment and multiple test sequences	PO4(3), PO6(3), PO7(2)	3	3

Programme Elective courses

VL25001	VLSI Signal Processing	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ul style="list-style-type: none"> To introduce techniques for altering existing DSP structures to suit VLSI implementations. To introduce efficient design of DSP architectures suitable for VLSI. 					
<p>Introduction to DSP Systems, Pipelining and Parallel Processing of Fir Filters Introduction to DSP systems – typical DSP algorithms, data flow and dependence graphs – critical path, loop bound, iteration bound, longest path matrix algorithm, pipelining and parallel processing of FIR filters, pipelining and parallel processing for low power.</p> <p>Retiming, Algorithmic Strength Reduction: Retiming – definitions and properties, unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even, Merge-Sort architecture, parallel rank-order filters.</p> <p>Fast Convolution, Pipelining And Parallel Processing of IIR Filters: Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.</p> <p>BIT-Level Arithmetic Architectures: Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters</p> <p>Numerical Strength Reduction, Synchronous and Asynchronous Pipelining Numerical strength reduction – sub-expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining - Bundled Data versus Dual-Rail protocol.</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References:</p> <ol style="list-style-type: none"> Keshab K. Parhi, “ VLSI Digital Signal Processing Systems, Design and Implementation “, Wiley, Interscience, 2007 U. Meyer – Baese, “ Digital Signal Processing with Field Programmable Gate Arrays”, Springer, 2nd Edition, 2004. 					

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand DSP algorithms, data flow graphs, critical path, iteration bound, and pipelining techniques for FIR and IIR filters	-	-	-
CO2	Apply retiming, unfolding, and algorithmic strength reduction to optimize DSP architectures for VLSI implementation	PO2(3), PO3(3), PO5(2)	3	3
CO3	Design and implement fast convolution, parallel processing, and bit-level arithmetic architectures for FIR/IIR filters	PO3(3), PO4(3), PO5(2)	3	3
CO4	Analyze and implement synchronous and asynchronous pipelining techniques, numerical strength reduction, and distributed arithmetic in DSP systems	PO4(3), PO6(3), PO7(2)	3	3

EL25C04	RF Integrated Circuit Design	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <p>To study CMOS transceiver design, noise analysis, impedance matching, amplifier and feedback system design, mixers, oscillators, and frequency synthesizers for high-performance communication systems.</p>					
<p>CMOS Physics, Transceiver Specifications and Architectures</p> <p>Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up conversion Transmitter, Two step up conversion Transmitter.</p> <p>Activity: Analysis of CMOS Transceiver Architectures and Noise Performance in Communication Systems</p>					
<p>Impedance Matching and Amplifiers</p> <p>S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.</p> <p>Activity: Design and Analyze a Source-Degenerated Common-Source LNA Using S-Parameters and Smith Chart–Based Impedance Matching</p>					
<p>Feedback Systems and Power Amplifiers</p> <p>Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model — Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations</p> <p>Activity: Analyze Stability, Efficiency, and Linearity in Class A–F Power Amplifiers Using Gain/Phase Margin, Root-Locus, and ACPR Evaluation</p>					
<p>Mixers and Oscillators</p> <p>Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.</p> <p>Activity: Analyze and Compare Mixer Architectures and Oscillator Designs Using Nonlinear Characteristics, Describing Functions, and Phase-Noise Evaluation</p>					

PLL and Frequency Synthesizers

Linearized Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

Activity: Model and Evaluate a PLL-Based Integer-N Frequency Synthesizer Using Linearized Loop Analysis, Noise Characterization, and Phase-Detector/Charge-Pump Design

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References

1. Lee, T. (2004). Design of CMOS RF integrated circuits. Cambridge University Press.
2. Razavi, B. (2013). RF microelectronics (2nd ed.). Pearson Education.
3. Crols, J., & Steyaert, M. (1997). CMOS wireless transceiver design. Kluwer Academic Publishers.
4. Razavi, B. (2017). Design of analog CMOS integrated circuits (2nd ed.). McGraw-Hill Education.
5. Indian Institute of Technology Madras. (n.d.). EE6240 – Recorded lectures and notes. <http://www.ee.iitm.ac.in/~ani/ee6240/>

	CO description	PO Mapping	PSO1	PSO2
CO1	understand user specifications for RF systems	-	-	-
CO2	design RF low noise amplifiers, power amplifiers, RF mixers and oscillators	PO3(3)	3	2
CO3	Analyze PLL for RF applications	PO1(3)	3	2

EL25C05	Electromagnetic Interference and Compatibility	L	T	P	C
		3	0	0	3
<p>Course Objective: This course aims to equip students with a comprehensive understanding of Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC), enabling them to identify and analyze EMI sources and coupling mechanisms, apply effective mitigation techniques like shielding, grounding, and filtering, comprehend relevant national and international EMC standards and regulations, and gain practical knowledge of EMI/EMC test methods and instrumentation, ultimately allowing them to design electromagnetically compatible electronic systems and PCBs.</p>					
<p>Introduction to EMI & EMC Definitions and Concepts – EMC Environment - EMC Testing Categories - Basic Electromagnetic Theory: Maxwell's equations and their application in EMC, Near-field and far-field approximations, Concepts of impedance</p> <p>Activity 1: EMI Source Identification & Classification Activity 2: Near-Field vs Far-Field Exploration Using Simple Calculations</p>					
<p>EMI Coupling Mechanisms Coupling Paths - basic coupling mechanisms: Conducted Coupling, Capacitive Coupling, Inductive/Magnetic Coupling, Radiative / Electromagnetic Coupling – Crosstalk - Transient Sources - Automotive transients.</p> <p>Activity 1: Identify and Classify EMI Coupling Mechanisms in Real Devices Activity 2: Hands-On Demonstration of Crosstalk and Transient Effects</p>					
<p>EMI Mitigation Techniques & EMC Standards Shielding – Grounding – Filtering – Cabling – Bonding - Need for Standards - National and International EMC Standardizing Organizations: IEC, FCC, CISPR, ANSI, BSI, CENELEC, ETSI - Key Standards and Specifications: MIL-STD, Electro Magnetic Emission and Susceptibility standards.</p> <p>Activity 1: EMI Mitigation Hands-On Experiment Activity 2: EMC Standards Research & Presentation</p>					
<p>EMI Test Methods and Instrumentation Fundamental Considerations - Emission Testing: Conducted Emissions, Radiated Emissions - Immunity/Susceptibility Testing: Conducted Immunity, Radiated Immunity, ESD Testing, Transient Immunity - Test Equipment</p> <p>Activity 1: Emission Testing Demonstration Activity 2: Immunity and ESD Testing Simulation</p>					
<p>PCB Design for EMC Compliance PCB Layout and Stack-up - Signal Integrity Considerations - Mixed-Signal PCB Layout: Grounding and power distribution for mixed-signal systems, Isolation of sensitive circuits - Component Placement for EMC</p> <p>Activity 1: Analyzing PCB Layout for EMC Issues Activity 2: Design a Simple EMC-Compliant PCB Section</p>					

References:

1. Ott, H. W. (1988). *Electromagnetic compatibility engineering* (2nd ed.). John Wiley & Sons.
2. Paul, C. R. (2010). *Introduction to electromagnetic compatibility* (2nd ed.). Wiley Interscience.
3. Ott, H. W. (1988). *Noise reduction techniques in electronic systems* (2nd ed.). John Wiley & Sons.
4. Keiser, B. (1989). *Principles of electromagnetic compatibility* (3rd ed.). Artech House.
5. Kodali, V. P. (2001). *Engineering electromagnetic compatibility: Principles, measurements, and technologies with computer models* (2nd ed.). IEEE Press.

E-Resources:

1. [http:// www.ewh.ieee.org/soc/emcs/](http://www.ewh.ieee.org/soc/emcs/)
2. <https://archive.nptel.ac.in/courses/108/106/108106138/>
3. <https://nptel.ac.in/courses/108106138>
4. https://onlinecourses.nptel.ac.in/noc24_ee67/preview

Weightage: Continuous Assessment: 40%, **End Semester Examinations:** 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Identify, categorize, and explain various sources of electromagnetic interference and EMC testing categories and EMI/EMC test methods, recognize the associated instrumentation, and critically evaluate test results for compliance.	-	-	-
CO2	Analyze and classify the coupling mechanisms (conducted, radiated, capacitive, inductive), and their impact on electronic systems.	PO3(3)	2	3
CO3	Integrate EMC principles into the design process of electronic circuits and printed circuit boards (PCBs), optimizing layouts, component placement, and power/ground distribution to ensure inherent electromagnetic compatibility.	PO1(3) PO(2)	2	3

VL25002	Physical Design of VLSI	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ul style="list-style-type: none"> • Understand the Basics of physical design flow such as component placement, floorplan, routing area partitioning • Study the concepts of algorithms used for optimization and how to apply this algorithm in placement and routing • Discuss the Detailed and specialized routing and relevant algorithm • Understand the concepts of Compaction • Study the some knowledge on VLSI Design Automation 					
<p>Introduction to VLSI Physical Design Flow: Circuit partitioning, placement and routing algorithms. Design Rule-verification, Circuit Compaction; Circuit Extraction and post layout simulation. FPGA design flow- partitioning, placement and routing algorithms. Deep sub-micron issues; interconnects modelling and synthesis.</p> <p>Placement and Routing: Global Placement and Routing: Introduction and objectives of placement, Global placement algorithms: min-cut placement, analytic placement, simulated annealing, Modern placement algorithms Routing terminology and goals. Dijkstra's algorithm. Global routing in a connectivity graph, Modern global routing, over the cell routing algorithms</p> <p>Detailed and Specialized Routing: Building the Horizontal and Vertical Constraint Graphs, Left edge algorithm, dog-legging, Switchbox routing, Introduction to area routing, Non-Manhattan routing, Routing in clock networks, clock-tree synthesis.</p> <p>Compaction: Basic definitions: One-dimensional mask layout compaction. Constraint graph. Circuit extraction and design rule checking. One-dimensional constraint graph compaction algorithm. Two-dimensional compaction, Recent trends in Compaction.</p> <p>VLSI Design Automation: VLSI design automation tools- algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References:</p> <ol style="list-style-type: none"> 1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1998. 2. N.A.Sherwani, "Algorithms for VLSI Physical Design Automation", (3/e), Kluwer, 1999. 3. Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure", 1st Edition, Springer, 2011 4. Sadiq M Sait and Habib Youssef, "VLSI Physical Design Automation", 1st Edition, World Scientific Publishing, 1995 					

5. S.M. Sait, H. Youssef, "VLSI Physical Design Automation", World scientific, 1999.
6. M.Sarrafzadeh, "Introduction to VLSI Physical Design", McGraw Hill (IE), 1996.
7. Michael S. Smith: Application Specific Integrated Circuits, Addison-Wesley, 1997
8. Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.

E-resources:

[https://en.wikipedia.org/wiki/Physical_design_\(electronics\)](https://en.wikipedia.org/wiki/Physical_design_(electronics))

<https://www.ifte.de/books/eda/chapl.pdf>

<https://nptel.ac.in/courses/106/105/106105161/>

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand the VLSI physical design flow, including placement, routing, compaction, and post-layout simulation	-	-	-
CO2	Apply algorithms for placement and routing such as min-cut, analytic placement, simulated annealing, and Dijkstra's algorithm	PO2(3), PO3(3), PO5(2)	3	3
CO3	Analyze detailed and specialized routing techniques including switchbox routing, clock-tree synthesis, and non-Manhattan routing	PO3(3), PO4(3), PO5(2)	3	3
CO4	Utilize compaction methods and VLSI design automation tools for efficient layout design and verification	PO4(3), PO6(3), PO7(2)	3	3

AP25C06	Hardware / Software Co-Design	L	T	P	C
		3	0	0	3
Course Objectives:					
<p>The objective of this course is to acquire the knowledge about system specification and modeling and to learn the formulation of partitioning. This course also deals with the different technical aspects about prototyping, emulation and verification.</p>					
System Specification and Modelling					
<p>Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification And Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures With One ASIC, Single-Processor Architectures With Many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification.</p>					
Hardware/Software Partitioning					
<p>The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.</p>					
Hardware/Software Co-Synthesis					
<p>The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis – Hardware/software co-synthesis algorithms: hardware – software partitioning, distributed system co-synthesis.</p>					
Prototyping and Emulation					
<p>Introduction, Prototyping And Emulation Techniques, Prototyping and Emulation Environments, Future Developments In Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.</p>					
Design Specification and Verification					
<p>Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design: System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-Simulation</p>					
References:					
<ol style="list-style-type: none"> 1. Schaumont, P. (2010). A practical introduction to hardware/software codesign. Springer. 2. Niemann, R. (1998). Hardware/software co-design for data flow dominated embedded systems. Kluwer Academic Publishers. 					

3. Staunstrup, J., & Wolf, W. (1997). Hardware/software co-design: Principles and practice. Kluwer Academic Publishers.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Describe the broad range of system architectures and design methodologies that currently exist and define their fundamental attributes.	-	-	-
CO2	Apply the dataflow models as a state-of-the-art methodology to solve co-design problems and to optimize the balance between software and hardware	PO3(3)	2	3
CO3	Develop co-design solutions to problems using modern hardware/software tools for building prototypes.	PO1(3)	3	3
CO4	Identify the concurrent specification from an algorithm, analyze its behavior and partition the specification into software and hardware components	PO1(3) PO(2)	2	3

VL25003	CAD for VLSI Design	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ul style="list-style-type: none"> • To introduce the VLSI design methodologies and design methods. • To introduce data structures and algorithms required for VLSI design. • To study algorithms for partitioning and placement. • To study algorithms for floor planning and routing. • To study algorithms for modelling, simulation and synthesis 					
<p>Introduction Introduction to VLSI Design Methodologies - VLSI Design Cycle - New Trends in VLSI Design Cycle - Physical Design Cycle - New Trends in Physical Design Cycle - Design Styles - Review of VLSI Design Automation Tools</p>					
<p>Data Structures and Basic Algorithms Introduction to Data Structures and Algorithms - Algorithmic Graph Theory and Computational Complexity- General Purpose Methods for Combinatorial Optimization.</p>					
<p>Algorithms for Partitioning and Placement Layout Compaction - Problem Formulation - Algorithms for Constraint Graph Compaction - Partitioning - Placement - Placement Algorithms.</p>					
<p>Algorithms for Floor Planning and Routing Floor planning - Problem Formulation - Floor planning Algorithms - Routing - Area Routing - Global Routing- Detailed Routing</p>					
<p>Modelling, Simulation and Synthesis Simulation - Gate Level Modelling and Simulation - Logic Synthesis and Verification - Binary Decision Diagrams - High Level Synthesis</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand VLSI design methodologies, VLSI/physical design cycles, design styles, and CAD tools	-	-	-
CO2	Apply data structures and basic algorithms for VLSI design, graph theory, and combinatorial optimization	PO2(3), PO3(3), PO5(2)	3	3
CO3	Analyze algorithms for partitioning and placement including constraint graph compaction	PO3(3), PO4(3), PO5(2)	3	3
CO4	Apply floor planning and routing algorithms for area, global, and detailed routing	PO3(3), PO4(3), PO5(2)	3	3
CO5	Understand modelling, simulation, logic synthesis, high-level synthesis, and verification using BDDs	PO3(3), PO4(3), PO6(2)	3	3

VL25004	Nanotechnology	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ul style="list-style-type: none"> • Provides knowledge of various industrial applications of Nanotechnology • Introduces the theory and practice on Nanomaterials • Imparting the state of art of nanotechnology to the society and to the environmental implication • To exercise the students' knowledge and imagination of Nanoscience and nanotechnology toward engineering applications coupled with detailed justifications. 					
<p>Nanotechnology: Background, what is Nanotechnology, types of Nanotechnology and Nano-machines, top down and bottom up techniques, atomic manipulation-Nanodots, semi-conductor quantum dots, self- assembly monolayers, simple details of characterization tools- SEM, TEM, STM, AFM.</p>					
<p>Nanomaterials: What are Nanomaterials? Preparation of Nanomaterials- solid state reaction method, Chemical Vapor Deposition, SOL-GELS techniques, electrodeposition, ball milling, introduction to lithography, Pulse Laser Deposition (PLD), applications of Nanomaterials</p>					
<p>Carbon Tubes: New forms of carbon, carbon tubes-types of Nanotubes, formation of Nanotubes, assemblies, purification of carbon Nanotubes, properties of Nanotubes, applications of Nanotubes</p>					
<p>Optics, Photonics and Solar Energy: Light and Nanotechnology, interaction of light and Nanotechnology, Nanoholes and photons, solar cells, optically useful Nanostructured polymers, photonic crystals.</p>					
<p>Future Applications: MEMS, Nanomachines, Nanodevices, Quantum Computers, Opto-electronic Devices, Quantum Electronic devices, environmental and biological applications.</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References</p> <ol style="list-style-type: none"> 1. Mick Wilson, Kamali Kannangra Geoff Smith, Michelle Simons and Burkhard Raguse, "Nanotechnology-Basic Science and Emerging Technologies", Overseas Press, 2002 2. Mark Ratner and Daniel Ratner, "Nanotechnology-a Gentle Introduction to The Next Big Idea", Prentice Hall, 2003 3. Rebecca L Johnson, "Nanotechnology", Lerner Publications, 2003 4. Charles P. Poole Jr., "Introduction to Nanotechnology", Chapman and Hall/CRS, 2003 					

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand fundamentals of nanotechnology, types, nanoscale machines, and fabrication techniques	-	-	-
CO2	Explain theory, preparation, and characterization of nanomaterials (SEM, TEM, STM, AFM)	PO1(3), PO3(3), PO5(2)	3	3
CO3	Understand properties, types, and applications of carbon nanotubes	PO1(3), PO2(2), PO3(2)	3	2
CO4	Explore optics, photonics, solar energy, MEMS, nanomachines, quantum devices, and societal/biological applications	PO1(3), PO2(2), PO4(3), PO6(2)	3	3

VL25005	Pattern Recognition	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ul style="list-style-type: none"> • To understand basic concepts in pattern recognition • To understand and analyze the different pattern recognition algorithms. • To familiarize about different pattern estimation methods. • To explore the role of Hidden Marko model and SVM in pattern recognition. • To understand the application of Fuzzy logic and genetic algorithms in real life. 					
<p>Pattern Classifier: Overview of Pattern recognition - Discriminant functions - Supervised learning - Parametric estimation - Maximum Likelihood Estimation - Bayesian parameter Estimation - Problems with Bayes approach- Pattern classification by distance functions - Minimum distance pattern classifier.</p>					
<p>Unsupervised Learning and Clustering: Criterion functions for clustering, Clustering Techniques: Iterative Square - error partitional clustering -K means with problems, hierarchical clustering, Graph theoretic approach to pattern Clustering, Cluster validation.</p>					
<p>Parameter Estimation Methods: Maximum-Likelihood estimation, Bayesian Parameter estimation, Dimension reduction methods - Principal Component Analysis (PCA}, Fisher Linear discriminant analysis, Expectation -maximization (EM}, Hidden Markov Models (HMM}.</p>					
<p>Non Parametric Techniques: Density Estimation, Parzen Windows, K-Nearest Neighbor Estimation, Nearest Neighbor Rule, Fuzzy classification.</p>					
<p>Recent Advances: Neural network structures for Pattern Recognition, Unsupervised learning in neural Pattern Recognition, Case Study Using Fuzzy Pattern Classifiers and Perception related to Web Applications - Audio and Video Analysis - Medical Applications - Image processing, Pattern classification using Genetic Algorithms.</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References:</p> <ol style="list-style-type: none"> 1. Richard O. Duda, Peter E. Hart and David G. Stork, "Pattern Classification", 2nd Edition, John Wiley, 2006. 2. C. M. Bishop, "Pattern Recognition and Machine Learning", Springer, 2009. 3. S. Theodoridis and K. Koutroumbas, "Pattern Recognition", 4th Edition, Academic Press, 2009. 4. Robert J. Schalkoff, Pattern Recognition Statistical, Structural and Neural Approaches, John Wiley & Sons Inc., New York, 1992. 5. Tou and Gonzales, Pattern Recognition Principles, Wesley Publication Company, London, 1974. 					

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand the fundamentals of nanotechnology, types, and nano-machines	-	-	-
CO2	Analyze preparation methods of nanomaterials, including chemical and physical techniques	PO2(3), PO3(3), PO5(2)	3	3
CO3	Understand carbon nanotubes, their properties, purification methods, and applications	PO3(3), PO4(3), PO5(2)	3	3
CO4	Explore applications in optics, photonics, solar energy, MEMS, nanodevices, and future technology	PO3(3), PO4(3), PO6(2)	3	3

AP25C05	Signal Integrity for High Speed Design	L	T	P	C
		3	0	0	3
<p>Course Objective: The objective of this course is to introduce students to the principles and challenges of maintaining signal integrity in high-speed digital designs. It aims to provide a comprehensive understanding of transmission line behavior, impedance control, reflections, crosstalk, differential signaling, and clock distribution. The course emphasizes practical analysis, modeling, and mitigation techniques used in designing robust and reliable high-speed digital systems.</p>					
<p>Introduction Introduction to Signal Integrity, Signal Quality on a Single Net, Cross Talk, Rail-Collapse Noise, Electromagnetic Interference (EMI), Signal-Integrity Solutions in Terms of Impedance: Impedance of ideal resistor, capacitor and inductor in time domain, Impedance in the Frequency Domain, Bulk Resistivity, Resistance per Length, Sheet Resistance, Power and Ground Planes and Decoupling Capacitance, Capacitance per Length, Self-Inductance and Mutual Inductance, Partial Inductance Effective, Total, or Net Inductance and Ground Bounce, Loop Self- and Mutual Inductance, Loop Inductance per Square of Planes, Loop Inductance of Planes and Via Contacts</p> <p>Activity:</p> <ol style="list-style-type: none"> Simulation Assignment: Use EDA tools like LTspice to simulate impedance mismatch and analyze signal degradation on a PCB trace. Poster Presentation: Students prepare a poster explaining impedance behavior in the time vs frequency domain, and the concept of ground bounce and EMI. 					
<p>Transmission Lines and Reflections</p> <p>Speed of a Signal in a Transmission Line, Instantaneous Impedance of a Transmission Line, Characteristic Impedance and Controlled Impedance, Return Paths , Frequency Variation of the Characteristic Impedance, Reflections, Reflections from Resistive Loads, Source Impedance, Bounce Diagrams, Reflections from Short Series and Short-Stub Transmission Lines, Reflections from Capacitive End Terminations, Reflections from Capacitive Loads in the Middle of a Trace, Capacitive Delay Adders, Effects of Corners and Vias, Loaded Lines, Reflections from Inductive Discontinuities, Compensation, Losses in Transmission Lines, Sources of Loss: Conductor Resistance and Skin Depth, The Dielectric, Dissipation Factor</p> <p>Activity:</p> <ol style="list-style-type: none"> Flipped Classroom: Students review pre-recorded videos on reflection and impedance mismatch; classroom used for solving bounce diagram exercises. Hands-on Lab: Build and measure signal reflection and delay using a coaxial cable, function generator, and oscilloscope (or simulation-based equivalent). 					

Crosstalk

Coupling: Capacitance and Inductance, Cross Talk in Transmission Lines, Cross Talk in Uniform Transmission Lines and Saturation Length, Capacitively Coupled Currents, Inductively Coupled Currents, Near-End Cross Talk, Far-End Cross Talk, Decreasing Far-End Cross Talk, Guard Traces, Cross Talk and Dielectric, Cross Talk and Timing, Switching Noise.

Activity:

1. **Case Study Analysis:**Analyze real PCB designs or documented failures where crosstalk affected system reliability (e.g., DDR memory buses, HDMI lines).
2. **Mini Quiz / Diagram Exercise:** Conduct a quick in-class quiz identifying near-end and far-end crosstalk with diagram-based questions.

Differential Signaling

Differential Signaling, A Differential Pair, Differential Impedance with No Coupling, The Impact from Coupling, Calculating Differential Impedance, The Return-Current Distribution in a Differential Pair, Ideal Coupled Transmission-Line Model or an Ideal Differential Pair, Cross Talk in Differential Pairs, Crossing a Gap in the Return Path.

Activity:

1. **Simulation/Modeling Task:** Use EDA tools to model differential pairs and evaluate the effects of spacing and return path discontinuities.
2. **Group Presentation:** Students present on how differential signaling improves noise immunity and is used in USB, PCIe, or HDMI.

Clock Distribution and Clock Oscillators

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

Activity:

1. **Timing Budgeting Exercise:** Given a real-world high-speed system, students calculate skew, jitter, and timing margins for clock distribution.
2. **Seminar / Tech Talk :** Students present on advanced clocking techniques (e.g., PLLs, low-jitter buffers) and common clock distribution topologies.

References:

1. Bogatin, E. (Year). *Signal and power integrity simplified* (3rd ed.). Pearson.
2. Johnson, H., & Graham, M. (Year). *High speed digital design*. Prentice Hall.
3. Johnson, H. (Year). *High speed signal propagation*. Prentice Hall.

E-Resources

1. <https://www.youtube.com/watch?v=YFwHV2EMB2A>
2. <https://suddendocs.samtec.com/notesandwhitepapers/samtec-signal-integrity-handbook.pdf>
3. <https://www.youtube.com/watch?v=KkfKQDnWf20>
4. https://onlinecourses.nptel.ac.in/noc24_ee67/preview

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Understand the fundamental concepts of signal integrity and analyze the effects of impedance, capacitance, and inductance on signal quality in high-speed circuits.	-	-	-
CO2	Analyze transmission line behavior, identify causes of signal reflection, and apply impedance matching techniques to minimize reflections and losses.	PO3(3)	3	3
CO3	Examine the sources and effects of crosstalk in high-speed designs and propose methods to mitigate timing and noise-related issues.	PO1(3)	3	3
CO4	Understand and evaluate differential signaling concepts, including impedance calculation, coupling effects, and return current paths.	PO1(3) PO(2)	2	3

VL25006	Network On Chip	L	T	P	C
		3	0	0	3
<p>Course Objectives: The students should be made to:</p> <ul style="list-style-type: none"> • Understand the concept of Network - on - Chip • Learn router architecture designs • Study fault tolerance Network - on – Chip 					
<p>Introduction to NOC: Introduction to NOC – OSI Layer Rules in NOC - Interconnection Networks in Network-On-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality- of-Service Support</p>					
<p>Architecture Design: Switching Techniques and Packet Format - Asynchronous FIFO Design - GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design</p>					
<p>Routing Algorithm: Packet Routing-QOS, Congestion Control and Flow Control – Router Design – Network Link Design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing For 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms</p>					
<p>Test and Fault Tolerance of NOC: Design-Security in Networks-On-Chips-Formal Verification of Communications in Networks-On Chips-Test and Fault Tolerance For Networks-On-Chip Infrastructures-Monitoring Services For Networks-On-Chips</p>					
<p>Three-Dimensional Integration of Network-On-CHIP: Three-Dimensional Networks-On-Chips Architectures – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation For QOS On-Chip Communication – Networks-On-Chip Protocols-On-Chip Processor Traffic Modeling For Networks-On-Chip</p>					
<p>References:</p> <ol style="list-style-type: none"> 1. ChrysostoMOSnicopoulos, Vijaykrishnan Narayanan, Chita R.Das” Networks-On – Chip “ Architectures Holistic Design Exploration”, Springer. 2. Fayezegebali, Haythamelmiligi, Hqhahedwatheq E1-Kharashi “Networks-On-Chips Theory and Practice CRC Press 3. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-On-Chip Architectures” 2013 4. Palesi, Maurizio, Daneshtalab, Masoud “Routing Algorithms in Networks-On-Chip” 2014 					
<p>E-resources:</p> <ol style="list-style-type: none"> 1. https://www.nasa.gov/smallsat-institute/sst-soa/thermal-control/ 2. https://ntrs.nasa.gov/api/citations/20230013900/downloads/NASA%20Thermal%20Control%20Engineering%20Guidebook%20v4.pdf 3. NIST Chemistry WebBook – Thermophysical Properties https://webbook.nist.gov/chemistry/ 					

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand the fundamentals of Network-on-Chip (NoC), interconnection networks, topologies, and OSI layer rules	-	-	-
CO2	Analyze router architecture designs including asynchronous FIFO, wormhole, VC, and adaptive routers	PO2(3), PO3(3), PO5(2)	3	3
CO3	Apply routing algorithms for NoC including packet routing, QoS, congestion control, multicast, and fault-tolerant routing	PO3(3), PO4(3), PO5(2)	3	3
CO4	Evaluate test methods, fault tolerance, verification, and monitoring in NoC and understand 3D NoC architectures	PO3(3), PO4(3), PO6(2)	3	3

VL25C01	VLSI For Wireless Communication	L	T	P	C
		3	0	0	3
<p>Course Objective:</p> <p>This Course Explores the principles and design methodologies for implementing wireless communication systems using VLSI. It focuses on rf front-end architectures, mixers, amplifiers, ADCS, and synthesizers, considering power, noise, and non-idealities. Emphasis is placed on practical implementation using modern VLSI techniques in CMOS technologies.</p>					
<p>Communication Systems & Wireless Channel Models</p> <p>Overview of Wireless Systems and Standards. TDMA, FDMA, CDMA, OFDMA. Modulation Schemes (BPSK, QPSK, MSK, OFDM). Classical And Wireless Channel Models – Path Loss, Multipath Fading, Doppler Spread, Coherence Bandwidth.</p> <p>Activity (Simulation):</p> <p>(I) Simulation of Wireless Channel and Modulation Schemes Using MATLAB. (ii) Ber Vs Snr Analysis Under AWGN And Fading Conditions.</p>					
<p>Receiver Architectures and LNA Design</p> <p>Receiver Types: Heterodyne, Homodyne, And Low-If. RF Front-End: Bandpass Filters, Noise Figure, Linearity, Gain. Wideband And Narrowband Lna Design, Matching Networks, NF Vs Power Trade-Off.</p> <p>Activity (EDA Tools):</p> <p>(I) Simulation AND Analysis of Gain, NF of A CMOS LNA. (ii) Impedance Matching Using Smith Chart.</p>					
<p>Mixer Design – Active and Passive</p> <p>Gilbert Cell Mixer, Conversion Gain, Distortion, Noise Figure, Lo-Rf Isolation. Switching Mixers, Sampling Mixers – Non-Idealities and Noise Analysis.</p> <p>Activity (Eda Tools):</p> <p>(I) Design and Simulation of Active Gilbert Mixer. (ii) Conversion Gain and NF Evaluation Using Spice.</p>					
<p>A/D Converters in Wireless Systems</p> <p>Demodulators And ADC Types: Flash, Pipeline, And Sigma-Delta. Band Pass Vs Low-Pass $\Sigma\Delta$ Modulators. Implementation With Switched-Capacitor Circuits. I/Q Mismatch.</p> <p>Activity (Simulation):</p> <p>(I) Modeling Of 1-Bit $\Sigma\Delta$ ADC In MATLAB/Simulink. (ii) System-Level Ber Analysis of ADC Output.</p>					

Frequency Synthesizers and Transmitters

PLL-Based Frequency Synthesizers, Phase Detectors, VCOS, Loop Filters. Phase Noise and Spur Analysis. Transmitter Architectures – Quadrature Lo Generation, Pa Design (Class A, B, E), Linearity, Output Control.

Activity (Eda Tools):

- (I) Design And Simulation of Ring Oscillator.
- (ii) Efficiency and Output Power Analysis of A Class E Pa.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review Of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Bosco Leung, *VLSI for Wireless Communication*, Second Edition, Springer, 2011.
2. BehzadRazavi, *RF Microelectronics*, Second Edition, Pearson, 2011.
3. BehzadRazavi, *Design of Analog CMOS Integrated Circuits*, Second Edition, McGraw-Hill, 2017.
4. K. K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Reprint, Wiley India, 2019.
5. Andreas F. Molisch, *Wireless Communications: From Fundamentals to beyond 5G*, Third edition, IEEE Press, 2022.

E-Resources

- <https://nptel.ac.in/courses/108106157> (RFIC Design)
- <https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/>
- <https://www.coursera.org/learn/rfic-design>
- <https://www.keysight.com> (Design guides for ADS)
- <https://www.ti.com/lit/ml/slyp173/slyp173.pdf> (RF Design for Wireless Communication)

	CO description	PO Mapping	PSO1	PSO2
CO1	Understand the Wireless System Blocks and Their Circuit-Level Implications.	-	-	-
CO2	Analyze and Design Front-End Receiver Components Like LNA And Mixers.	PO3(3)	3	2
CO3	Implement ADC Architectures AND Assess Their Performance for Wireless Systems.	PO1(3)	3	3
CO4	Develop And Simulate PLLS And Transmitter Components Including Pas.	PO1(3) PO(2)	2	3

VL25007	DSP Structures for VLSI	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ul style="list-style-type: none"> • to understand the fundamentals of DSP • to learn various DSP structures and their implementation. • to know designing constraints of various filters • design and optimize VLSI architectures for basic DSP algorithms • to enable students to design VLSI system with high speed and low power. • 					
<p>Introduction to Digital Signal Processing: Linear system theory- convolution- correlation - DFT- FFT- basic concepts in FIR filters and IIR filters- filter realizations. Representations of DSP algorithms- block diagram-SFG-</p> <p>Iteration Bound, Pipelining and Parallel Processing of Fir Filter: Data-flow graph representations- Loop bound and Iteration bound algorithms for computing iteration bound-LPM algorithm. Pipelining and parallel processing: pipelining of FIR digital filters- parallel processing, pipelining and parallel processing for low power.</p> <p>Retiming, Unfolding and Folding: Retiming: definitions, properties and problems-solving systems of inequalities. Properties of Unfolding, critical path, Unfolding and Retiming, applications of Unfolding, Folding transformation- register minimization techniques, register minimization in folded architecture- folding of multirate system.</p> <p>Fast Convolution: Cook-toom algorithm- modified cook-Toom algorithm. Design of fast convolution algorithm by inspection - Winograd algorithm- modified Winograd algorithm</p> <p>Arithmetic Strength Reduction in Filters: Parallel FIR filters-fast FIR algorithms-two parallel and three parallel. Parallel architectures for rank order filters -odd-even, merge-sort architecture-rank order filter architecture-parallel rank order filters-running order merge order sorter, low power rank order filter.</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review Of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References:</p> <ol style="list-style-type: none"> 1. K.K Parhi: "VLSI Digital Signal Processing", John-Wiley, 2nd Edition Reprint, 2008. 2. John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India, 1st Edition, 2009. 					

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand fundamentals of Digital Signal Processing including linear systems, convolution, correlation, DFT/FFT, FIR and IIR filters	-	-	-
CO2	Analyze data-flow graph representations, compute iteration bound, and implement pipelining and parallel processing for FIR filters	PO2(3), PO3(3), PO5(2)	3	3
CO3	Apply retiming, unfolding, and folding transformations for DSP systems including register minimization	PO3(3), PO4(3), PO5(2)	3	3
CO4	Design and implement fast convolution algorithms using Cook-Toom, Winograd and modified algorithms	PO3(3), PO4(3), PO6(2)	3	3
CO5	Apply arithmetic strength reduction techniques for parallel and low-power DSP filter architectures	PO3(3), PO4(3), PO6(2)	3	3

VL25C02	MEMS & NEMS	L	T	P	C
		3	0	0	3
<p>Course Objective:</p> <ul style="list-style-type: none"> • To understand MEMS fundamentals and fabrication processes. • To impart knowledge of the photolithographic process, photo resist and pattern transfer. • To provide a fundamental of NEMS and its fabrication methods. • To explore carbon-based NEMS materials and fabrication challenges. • To learn about the diverse applications of MEMS and NEMS. 					
<p>Fundamentals of MEMS</p> <p>MEMS Introduction - Low Cost - Redundancy and Disposability – Scaling – Made – Substrates –Processing – Mask – Developing – Etching - Road Map and Perspective Silicon Substrate – Silicon Growth – Crystal - Miller Indices – Semiconductor – Doping - Additive Techniques.</p> <p>Activity:</p> <ul style="list-style-type: none"> • Case Study: Analyze the evolution and cost benefits of MEMS in healthcare diagnostics. • Hands-on: Silicon wafer orientation and doping simulation using open tools (e.g., NanoHUB). 					
<p>Pattern Transformation of Mems</p> <p>Photolithographic Process - Clean room - Photo Resist - Positive Resist - Negative Resist –Working with Resist – Applying Photo Resist - Exposure and Pattern Transfer - Printing Methods – Contact Proximity – Projection Printing - Development and Post Treatment -Masks – Resolution –Sensitivity and Resist Profiles – Mask Alignment - Permanent Resists</p> <p>Activity:</p> <ul style="list-style-type: none"> • Lab Demo / Video Simulation: Lithography and mask alignment procedure • Assignment: Design a basic mask layout for a MEMS pattern 					
<p>Introduction of NEMS</p> <p>Introduction – Basic properties - Benefits of Nanomachines – Miniaturization - NEMS Memory – Importance of AFM - Top-Down Approach - NEMS devices - NEMS Advantages.</p> <p>Activity:</p> <ul style="list-style-type: none"> • Seminar: Benefits and miniaturization challenges in NEMS • Simulation: NEMS memory modeling using nano-electronics simulator (NanoHub toolkit) 					
<p>Feedback Amplifiers and Waveform Generators</p> <p>Materials – Carbon Allotropes - Carbon Based Materials - Metallic Carbon Nanotubes – Difficulties – Simulations - Current Challenges and future of NEMS – Deposition processes – Lithography – Etching processes.</p> <p>Activity:</p> <ul style="list-style-type: none"> • Group Project: Design and simulate a carbon nanotube-based NEMS device • Quiz: On lithography types and carbon-based nanomaterials 					

Power Amplifiers

Pressure sensor - Piezoresistive sensor - Capacitive sensor – RF applications – Gyroscope – Optical MEMS - Optical Data - Switching - RF MEMS - MEMS switches - MEMS Resonators. Case study: Cantilever piezoelectric actuator, Capacitive accelerometer, Piezoresistive pressure sensor

Activity:

- Case Study Presentation: Comparison of MEMS gyroscope and accelerometer
- Assignment: Technical report on emerging RF MEMS switches.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Explain the fundamentals of MEMS including materials, silicon substrates, fabrication processes, scaling concepts, and applications in sensing and actuation.	-	-	-
CO2	apply photolithographic and pattern transfer processes for MEMS device fabrication, including mask design and resist processing.	PO3(3)	3	2
CO3	Analyze the principles, materials, fabrication challenges, and performance of NEMS devices including carbon-based nanomaterials and feedback-based nanodevices.	PO1(3)	3	2
CO4	Design and evaluate MEMS/NEMS-based sensors, actuators, and RF/optical MEMS devices using simulations and case studies.	PO1(3) PO(2)	2	3

VL25008	Advanced Transistor Modelling	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ul style="list-style-type: none"> To acquire fundamental knowledge and to expose to the field of semiconductor theory and devices and their applications. To gain an adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications To acquire the fundamental knowledge of different semiconductor device modelling aspects. 					
<p>Fundamentals Of Semiconductors and Moscapacitors</p> <p>Equilibrium carrier concentration in intrinsic semiconductors, the Equilibrium carrier concentration in extrinsic semiconductors, Carrier transport in semiconductors Excess carriers in semiconductors, Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in a MOS Structure.</p> <p>Device Design</p> <p>MOSFET Scaling, Constant field scaling, Generalized scaling, Non-scaling effects, Threshold voltage, requirement Channel Profile Design, Non-uniform doping, Quantum effect on threshold voltage, Discrete dopant effects on threshold voltage MOSFET channel length, Extraction of effective channel length by C-V measurements.</p> <p>Mathematical Techniques for Device Characterization</p> <p>Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.</p> <p>Device Modelling</p> <p>SQEBASTIP -Nine Step Device Modelling procedure for P-N Junction, MOS Field Effect Transistor and Bipolar Junction Transistor</p> <p>FINFET Design</p> <p>I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References:</p> <ol style="list-style-type: none"> Yuan Taur and TakH.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016. 					

2. B.G Streetman and S.K Banerjee, "Solid State Electronic Devices", 7th edition, Prentice Hall India, 2010.
3. A.B. Bhattacharyya "Compact MOSFET Models for VLSI Design", John Wiley & Sons Ltd, 2009.
4. P. Colinge, "FinFETs and Other Multi-Gate Transistors", Springer. 2009
5. Ansgar Jungel, "Transport Equations for Semiconductors", Springer, 2009
6. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, "Device Modelling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd, 2004
7. Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer-Verlag., 1984
8. Behzad Razavi, "Fundamentals of Microelectronics" Wiley Student Edition, 2nd Edition, 2014
9. J P Collinge, CA Collinge, "Physics of Semiconductor devices" Springer, 2002. S.M.Sze, Kwok.K. NG, "Physics of Semiconductor devices", Springer, 2006.
10. S. Karmalkar, NPTEL Video lectures on Solid State Devices and their Transcripts available at: <http://nptel.ac.in/courses/117106091/>
11. S. Karmalkar, NPTEL Video lectures on Semiconductor Device Modeling available at: <http://nptel.ac.in/courses/117106033/>

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand fundamental concepts of semiconductors, carrier transport, and MOS capacitors	-	-	-
CO2	Analyze device design aspects including MOSFET scaling, threshold voltage, channel profiling, and non-uniform doping effects	PO2(3), PO3(3), PO5(2)	3	3
CO3	Apply mathematical techniques for semiconductor device characterization including Poisson, continuity, drift-diffusion, and Schrodinger equations	PO3(3), PO4(3), PO5(2)	3	3
CO4	Model semiconductor devices using structured device modeling procedures for PN junctions, MOSFETs, and BJTs	PO3(3), PO4(3), PO6(2)	3	3
CO5	Understand FinFET and GAA device design, device capacitances, parasitic effects, and novel circuit applications	PO3(3), PO4(3), PO6(2)	3	3

VL25009	VLSI Architectures for Image Processing	L T P C 3 0 0 3
Course Objectives:		
<ul style="list-style-type: none"> • The students will be able to acquire knowledge on image and video processing algorithms • The students will be able to acquire knowledge on design of VLSI architectures. 		
Image Processing Algorithms and Architectures		
Image Processing Tasks - Low Level Image Processing Operations - Intermediate Level Operations Image Processor Architecture: Requirements and Classification - Uni and Multi Processors - MIMD Systems - SIMD Systems - Pipelines - Design Aspects of Real Time Low Level Image Processors - Design Method for Special Architectures		
3D Image Processing		
Overview of 3D Image - Types and Characteristics of 3D Image Processing - Examples of 3D Image Processing, Continuous and Digitized Images, Models of Image Operations, Algorithm of Image Operations - Smoothing Filter - Difference Filter - Differential Features of a Curved Surface - Region Growing.		
3D Binary Image Processing		
Introduction- Labeling of a Connected - Shrinking- Surface Thinning and Axis Thinning- Distance Transformation and Skeleton-Border Surface Following-Knot and Link .- Voronoi Division of a Digitized Image-Algorithms for Processing Connected Components with Gray Values		
Pipelined, 2D and 3D Image Processing Architectures		
Architecture of a Cellular Logic Processing Element - Second Decomposition in Data Path and Control - Real Time Pipeline for Low Level Image Processing - Design Aspects of Image Processing Architectures - Implementation of Low Level 2D and 3D and Intermediate Level Algorithms		
VLSI Systems for Image Processing		
Concurrent Systems for Image Analysis- VLSI Wavefront Arrays for Image Processing- Curve Detection in VLSI-Design of VLSI Based Multicomputer Architecture for Dynamic Scene Analysis-VLSI-Based Image Resampling for Electronic Publishing		
Practical exercises:		
<ol style="list-style-type: none"> 1. Convert a 2D Image to 3D Image. 2. Perform Unary, Binary Image Operations and Monotonic, Shift, Point, Shift-Invariant Operators for 2D Image. 3. Obtain a CT Scan Image , Perform The Following <ol style="list-style-type: none"> a. Smooth Filter b. Detection Filter c. Morphological Filter d. Region Growing 4. Perform Surface Thinning and Axis Thinning, Distance Transformation and Skeleton, Voronoi Division of a Digitized Image 		
Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%		
Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).		

References

1. Pieter Jonker, "Morphological Image Processing: Architecture and VLSI Design", Springer, First Edition, 1992.
2. Junichiro Toriwaki · Hiroyuki Yoshida, "Fundamentals of Three-Dimensional Digital Image Processing", Springer 2009.
3. King-Sun Fu, "VLSI for Pattern Recognition and Image Processing", Springer-Verlag, 1984.

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand low-level and intermediate image processing algorithms and their VLSI implementation requirements	-	-	-
CO2	Analyze 3D image processing algorithms, continuous and digitized image models, and filtering techniques	PO2(3), PO3(3), PO4(2)	3	3
CO3	Apply 3D binary image processing techniques including labeling, surface thinning, skeletonization, and Voronoi division	PO3(3), PO4(3), PO5(2)	3	3
CO4	Design pipelined 2D and 3D image processing architectures using cellular logic elements and low-level real-time pipelines	PO3(3), PO4(3), PO5(2)	3	3
CO5	Implement VLSI systems for concurrent image analysis, including wavefront arrays, curve detection, and multicomputer architectures	PO3(3), PO4(3), PO6(2)	3	3

VL25010	Reconfigurable Architecture	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ul style="list-style-type: none"> • The student shall develop an overview and deeper insight into the research and development that is underway to meet future needs of flexible processors • to learn the concepts of implementation, synthesis and placement of modules in reconfigurable architectures • to understand the communication techniques and System on Programmable Chip for reconfigurable architectures • to learn the process of reconfiguration management • to familiarize the applications of reconfigurable architectures 					
<p>Introduction General purpose computing – domain specific processors – Application Specific Processors – reconfigurable computing – fields of application – evolution of reconfigurable systems – simple Programmable Logic Devices – Complex Programmable Logic Devices – Field Programmable Gate Arrays – coarse grained reconfigurable devices.</p>					
<p>Implementation, Synthesis and Placement Integration – FPGA design flow – logic synthesis – LUT based technology mapping – modeling – temporal partitioning algorithms – offline and online temporal placement – managing device’s free and occupied spaces.</p>					
<p>Communication and SOPC Direct communication – communication over third party – bus based communication – circuit switching – Network on Chip – dynamic Network on Chip – System on a Programmable Chip – adaptive multi-processing on chip.</p>					
<p>Reconfiguration Management Reconfiguration – configuration architectures – managing the reconfiguration process – reducing configuration transfer time – configuration security.</p>					
<p>Applications FPGA based parallel pattern matching - low power FPGA based architecture for microphone arrays in Wireless Sensor Networks - exploiting partial reconfiguration on a dynamic coarse grained reconfigurable architecture – parallel pipelined OFDM baseband modulator with dynamic frequency scaling for 5G systems.</p>					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					
<p>References:</p> <ol style="list-style-type: none"> 1. Christophe Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer 2007. 2. Scott Hauck and Andre Dehon, “Reconfigurable Computing: The Theory and Practice of FPGA Based Computation”, Elsevier 2008 3. M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005. 4. Nikoloas Voros Et Al. “Applied Reconfigurable Computing: Architectures, Tools and Applications” Springer, 2018. 					

5. Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, "Reconfigurable Computing: Architectures and Applications", Springer 2006.

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand concepts of reconfigurable computing, domain-specific and application-specific processors, and FPGA technologies	-	-	-
CO2	Apply techniques for implementation, synthesis, LUT-based mapping, and placement of modules in reconfigurable architectures	PO3(3), PO4(3), PO5(2)	3	3
CO3	Analyze communication techniques including direct, bus-based, circuit switching, and Network-on-Chip in reconfigurable systems	PO3(3), PO4(3), PO5(2)	3	3
CO4	Understand reconfiguration management, configuration architectures, security, and optimization of configuration transfer	PO3(3), PO4(3), PO6(2)	3	3
CO5	Explore applications of reconfigurable architectures in FPGA-based systems, parallel processing, and 5G baseband processing	PO3(3), PO4(3), PO5(2)	3	3

VL25011	Adaptive Signal Processing	L	T	P	C
		3	0	0	3
Course Objectives: <ul style="list-style-type: none"> • to understand the basic principles of discrete random signal processing • to understand the principles of spectral estimation • to learn about the weiner and adaptive filters • to understand the different signal detection and estimation methods • to acquire skills to design synchronization methods for proper functioning of the system 					
Discrete Random Signal Processing Discrete Random Processes, Random Variables, Parseval's Theorem, Wiener-Khintchine Relation, Power Spectral Density, Spectral Factorization, Filtering Random Processes, Special Types of Random Processes					
Spectral Estimation Introduction, Nonparametric Methods – Periodogram, Modified Periodogram, Bartlett, Welch and Blackman-Tukey Methods, Parametric Methods – ARMA, AR and MA Model Based Spectral Estimation, Solution Using Levinson-Durbin Algorithm.					
Weiner and Adaptive Filters Weiner Filter: FIR Wiener Filter, IIR Wiener Filter, Adaptive Filter: FIR Adaptive Filters – Steepest Descent Method- LMS Algorithm, RLS Adaptive Algorithm, Applications.					
Detection and Estimation Bayes Detection Techniques, Map, MI,– Detection of M-Ary Signals, Neymanpearson, Minimax Decision Criteria. Kalman Filter- Discrete Kalman Filter, The Extended Kalman Filter, Application.					
Synchronization Signal Parameter Estimation, Carrier Phase Estimation, Symbol Timing Estimator, Joint Estimation of Carrier Phase and Symbol Timing.					
Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%					
Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).					
References: <ol style="list-style-type: none"> 1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc, Singapore, 2009. 2. John G. Proakis., "Digital Communication", 4th Edition, McGraw Hill Publications, 2001. 3. Simon Haykin, "Adaptive Filter Theory", Pearson Education, Fourth Edition, 2003 4. Bernard Sklar and Pabitra Kumar Roy, "Digital Communications: Fundamentals and Applications", 2/E, Pearson Education India, 2009 					

5. Paulo S. R. Diniz, "Adaptive Filtering Algorithms and Practical Implementation", Springer, 2011

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand basic principles of discrete random signal processing, random variables, and power spectral density	-	-	-
CO2	Apply spectral estimation techniques using nonparametric and parametric methods including periodogram and ARMA models	PO3(3), PO4(3), PO5(2)	3	3
CO3	Analyze and design Wiener filters and adaptive filters including LMS and RLS algorithms for signal processing applications	PO3(3), PO4(3), PO5(2)	3	3
CO4	Understand signal detection and estimation techniques including Bayes detection, MAP, ML, Neyman-Pearson criteria, and Kalman filtering	PO3(3), PO4(3), PO6(2)	3	3
CO5	Design synchronization methods for communication systems including carrier phase and symbol timing estimation	PO3(3), PO4(3), PO5(2)	3	3

VL25C03	Digital Image and Video Processing	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <p>This course aims to provide an in-depth understanding of advanced concepts in digital image and video processing, with a strong focus on temporal analysis, motion estimation, and 3D reconstruction. Students will learn to apply state-of-the-art techniques in video compression, tracking, and deep learning-based analysis to solve real-world problems. By the end of the course, learners will be equipped to design and implement efficient image and video processing systems for applications such as surveillance, autonomous systems, and immersive media.</p>					
<p>Motion Estimation and Video Fundamentals</p> <p>Temporal vs. spatial image processing - Basics of video formation and representation (color video, interlaced vs. progressive) - Frame differencing and background subtraction - Block matching algorithms (Full Search, Three Step Search, Diamond Search) - Optical flow (Lucas-Kanade and Horn-Schunck methods) - Applications: surveillance, object tracking.</p> <p>Activity 1: Motion Estimation with OpenCV (Block Matching vs. Optical Flow) - Tools: OpenCV (Python), sample videos (e.g., from UCF101 dataset) - Task: Implement and compare block matching and optical flow algorithms (Lucas-Kanade & Farnebäck) on test videos. - Outcome: Analyze tracking performance under different motion types.</p> <p>Activity 2: Flipped Class + Mini Project on Background Subtraction Techniques - Tools: OpenCV, Code samples from GitHub - Task: Pre-class video lectures + in-class implementation of MOG2 and KNN background subtraction on surveillance footage. - Outcome: Comparative report and demonstration of real-time performance.</p>					
<p>Video Compression Standards and Techniques</p> <p>Temporal redundancy and inter-frame coding - Overview of video compression standards: MPEG-1/2/4, H.264/AVC, HEVC - Intra vs. inter coding, GOP structure - Motion compensation and entropy coding in video codecs - Scalable and Multiview video coding.</p> <p>Activity 1: Video Codec Analysis using FFmpeg - Tools: FFmpeg (open source), sample videos from Xiph.org Video Test Media - Task: Encode videos using H.264, MPEG-4, and HEVC. Evaluate size, PSNR, and SSIM. - Outcome: Compression efficiency report.</p> <p>Activity 2: Flipped Classroom on GOP Structure - Tools: Handbrake + OpenCV + Python - Task: Analyze Group of Pictures (GOP) in compressed video streams. - Outcome: Presentation on impact of GOP length and I/P/B frame configuration.</p>					
<p>3D Image Processing and Multiview Video</p> <p>Stereoscopic imaging and disparity map estimation - 3D reconstruction from multiple images - Structure from motion (SfM) - Multiview video systems and depth estimation - Applications in VR/AR and 3D television.</p> <p>Activity 1: Stereo Vision and Disparity Map Generation - Tools: OpenCV stereo block matching, Middlebury Stereo Dataset - Task: Compute disparity maps from stereo pairs and visualize depth. - Outcome: Depth map quality evaluation and report.</p>					

Activity 2: Structure from Motion (SfM) using COLMAP - Tools: COLMAP (open source SfM), ETH3D dataset - Task: Reconstruct sparse and dense 3D scenes from multiple views. - Outcome: 3D point cloud visualization and reconstruction accuracy analysis.

Advanced Image and Video Analysis

Video segmentation and object tracking (Kalman filter, mean-shift, particle filter) - Action and gesture recognition - Scene understanding and semantic segmentation - Face and emotion recognition in video - Deep learning applications: CNNs for video, 3D CNNs, RNNs/LSTMs.

Activity 1: Action Recognition using Pre-trained CNN-LSTM Models Tools: PyTorch or TensorFlow, UCF101 dataset - Task: Use pretrained 3D CNN + LSTM pipeline to classify video actions. - Outcome: Confusion matrix + model performance summary.

Activity 2: Seminar on Research Paper Reproduction - Task: Reproduce a recent CVPR/ICCV paper (e.g., Deep SORT, YOLOv7 tracking) using open-source codebases. - Outcome: Present implementation steps, results, and challenges faced.

Real-Time Processing and Applications

Real-time image/video processing architectures (GPU, FPGA) - Edge AI and deployment on embedded devices - High-speed video capture and analysis - Applications: autonomous driving, medical video analysis, drone surveillance - Case studies and open research challenges.

Activity 1: Real-Time Object Tracking using Jetson Nano / Raspberry Pi - Tools: OpenCV + YOLOv5 or MobileNet-SSD, webcam or real-world video - Task: Deploy real-time object tracker on edge device. - Outcome: Demonstrate live tracking with FPS metrics.

Activity 2: Industry Case Study + Application Prototype - Task: Case study discussion on a real-world use (e.g., medical video analysis or drone surveillance) + student prototype. - Tools: Custom project using open-source libraries (e.g., OpenMMLab) - Outcome: Presentation + demo + report.

References

1. Szeliski, R. (2022). *Computer vision: Algorithms and applications* (2nd ed.). Springer.
2. Bovik, A. C. (Ed.). (2020). *The essential guide to video processing* (2nd ed.). Academic Press.
3. Singh, R. (2023). *Digital image and video processing: Principles and algorithms* (1st ed.). McGraw-Hill Education.
4. Marques, O. (2019). *Practical image and video processing using MATLAB* (2nd ed.). Wiley.
5. Goodfellow, I., Bengio, Y., & Courville, A. (2021). *Deep learning* (2nd ed.). MIT Press.

E-Resources

1. NPTEL Course: Digital Image Processing by Prof. P.K. Biswas, IIT Kharagpur.
2. NPTEL Course: Computer Vision by Prof. S. Raman, IIT Gandhinagar.

3. OpenCV Tutorials: https://docs.opencv.org/4.x/d6/d00/tutorial_py_root.html.
4. Coursera Course: Applied Computer Vision with Deep Learning (DeepLearning.AI).

CMU Video Lectures: Computer Vision (16-720) on YouTube.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Analyze the temporal characteristics of video sequences and apply motion estimation techniques such as block matching and optical flow to detect and track motion.	-	-	-
CO2	Evaluate and implement modern video compression algorithms by evaluating temporal and spatial redundancies for efficient video coding.	PO3(3)	3	2
CO3	Create depth maps and perform 3D reconstruction from stereo or Multiview image sequences using structure-from-motion techniques.	PO1(3)	3	1
CO4	Apply machine learning and deep learning models to recognize actions, objects, and scenes in video sequences with temporal consistency.	PO1(3) PO(2)	2	3

VL25012	Evolvable Hardware	L	T	P	C
		3	0	0	3
<p>Course Objectives:</p> <ul style="list-style-type: none"> To study about the evolvable systems algorithms, multi-objective utility functions Understand the concepts of reliability, design-in redundancy, fault tolerance and defect tolerance Design of evolvable systems using Programmable Logic Devices (like FPGAs) and modular subsystems with identical components and generalized controller algorithms 					
<p>Introduction Traditional Hardware Systems and its Limitations, Evolvable Hardware, Characteristics of Evolvable Circuits and Systems, Technology-Extrinsic and Intrinsic Evolution offline and Online Evolution, Applications and Scope of EHW</p> <p>Evolutionary Computation Fundamentals of evolutionary algorithms, components of EA, variants of EA, Genetic Algorithms, genetic programming, evolutionary strategies, evolutionary programming, implementations – evolutionary design and optimizations, EHW – current problems and potential solutions</p> <p>Reconfigurable Digital Devices Basic architectures – Programmable Logic Devices, Field Programmable Gate Arrays (FPGAS), using reconfigurable hardware – design phase, execution phase, evolution of digital circuits</p> <p>Reconfigurable Analog Devices Basic architectures – Field Programmable Transistor Arrays (FPTAS), analog arrays, MWMS, using reconfigurable hardware – design phase, execution phase, evolution of analog circuits</p> <p>Applications of EHW Synthesis vs. Adaptation, designing self-adaptive systems, fault-tolerant systems, real-time systems, intrinsic reconfiguration for online systems, EHW based fault recovery and future work</p>					
<p>References</p> <ol style="list-style-type: none"> Garrison W. Greenwood and Andrew M. Tyrrell, "Introduction to Evolvable Hardware: a Practical Guide for Designing Self- Adaptive Systems", Wiley-IEEE Press, 2006. Tetsuya Higuchi, Xin Yao and Yong Liu, "Evolvable Hardware", Springer-Verlag, 2004. Lukas Sekanina, "Evolvable Components: From Theory to Hardware Implementations", Springer, 2004 					
<p>Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%</p>					
<p>Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).</p>					

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand evolvable hardware systems, their characteristics, offline/online evolution, and applications	-	-	-
CO2	Apply evolutionary computation techniques including genetic algorithms, evolutionary strategies, and genetic programming for system design	PO3(3), PO4(3), PO5(2)	3	3
CO3	Design evolvable digital systems using reconfigurable devices like FPGAs, including design and execution phases	PO3(3), PO4(3), PO5(2)	3	3
CO4	Design evolvable analog systems using reconfigurable devices like FPTAs and analog arrays, including design and evolution of analog circuits	PO3(3), PO4(3), PO5(2)	3	3
CO5	Apply evolvable hardware concepts for real-time, self-adaptive, and fault-tolerant systems including intrinsic reconfiguration	PO3(3), PO4(3), PO6(2)	3	3