VISION

The Department of ECE shall strive continuously to create highly motivated, technologically competent engineers, be a benchmark and a trend setter in Electronics and Communication Engineering by imparting quality education with interwoven input from academic institutions, research organizations and industries, keeping in phase with rapidly changing technologies imbibing ethical values.

MISSION

- Imparting quality technical education through flexible student centric curriculum evolved continuously for students of ECE with diverse backgrounds.
- Providing good academic ambience by adopting best teaching and learning practices.
- Providing congenial ambience in inculcating critical thinking with a quest for creativity, innovation, research and development activities.
- Enhancing collaborative activities with academia, research institutions and industries by nurturing ethical entrepreneurship and leadership qualities.
- Nurturing continuous learning in the stat-of-the-art technologies and global outreach programmes resulting in competent world class engineers.
ANNA UNIVERSITY, CHENNAI
UNIVERSITY DEPARTMENTS
M.E. VLSI DESIGN
REGULATIONS - 2019

PROGRAMME EDUCATIONAL OBJECTIVES:

1. Teach students to understand the principles involved in the latest hardware and software required for designing and critically analyzing electronic circuits relevant to industry and society
2. Blend theory and laboratory to make students appreciate the concepts in the working of electronic circuits
3. Mould students to progress and develop with ethics and to communicate effectively
4. Motivate students to take up socially relevant and challenging projects and propose innovative solutions to problems for the benefit of the society
5. To motivate students to become entrepreneurs to develop indigenous solutions.

PROGRAM OUTCOMES:

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<tr>
<th>PO#</th>
<th>Graduate Attribute</th>
<th>Programme Outcome</th>
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<tr>
<td>1.</td>
<td>Research aptitude</td>
<td>An ability to independently carry out research/investigation and development work to solve practical problems</td>
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<td>2.</td>
<td>Technical documentation</td>
<td>An ability to write and present a substantial technical report/document</td>
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<td>3.</td>
<td>Technical competence</td>
<td>Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program</td>
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<td>4.</td>
<td>Engineering Design</td>
<td>An ability to apply various advanced tools and techniques to develop efficient Hardware solutions</td>
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<tr>
<td>5.</td>
<td>The engineer and society</td>
<td>Apply technical knowledge towards the development of socially relevant products</td>
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MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMME OUTCOMES:

A broad relation between the programme objective and the outcomes is given in the following table:

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<th>PEOs</th>
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* Audit Course is optional

**SEMESTER II**

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**THEORY**

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*(out of 6 courses one course must be selected)*

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## AUDIT COURSES (AC)
Registration for any of these courses is optional to students

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## EMPLOYABILITY ENHANCEMENT COURSES (EEC)

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OBJECTIVES:

- To encourage students to develop a working knowledge of the central ideas of linear algebra.
- To enable students to understand the concepts of probability and random variables.
- To make students understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete-time Markov chains.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in real life situation.
- To introduce the Fourier Transform as an extension of Fourier techniques on periodic functions and to solve partial differential equations.

UNIT I  
LINEAR ALGEBRA  

UNIT II  
ONE DIMENSIONAL RANDOM VARIABLES  

UNIT III  
RANDOM PROCESSES  
Classification – Auto correlation - Cross correlation - Stationary random process – Markov process — Markov chain - Poisson process – Gaussian process.

UNIT IV  
LINEAR PROGRAMMING  
Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

UNIT V  
FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS  

TOTAL: 45+15=60 PERIODS

COURSE OUTCOMES:
At the end of the course, students will be able to

- Apply the concepts of linear algebra to solve practical problems.
- Use the ideas of probability and random variables in solving engineering problems.
- Classify various random processes and solve problems involving stochastic processes.
- Formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
- Apply the Fourier transform methods of solving standard partial differential equations.

REFERENCES:
VL5152 DIGITAL CMOS VLSI DESIGN  L T P C
3 0 0 3

OBJECTIVES:
- To introduce the transistor level design of all digital building blocks common to all CMOS microprocessors, network processors, digital backend of all wireless systems etc
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption.

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER
MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter-Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, Stick diagram and Layout diagrams.

UNIT II COMBINATIONAL LOGIC CIRCUITS
Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Interconnect Delay, Dynamic Logic Gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS
Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Nonbistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS
Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs

UNIT V MEMORY ARCHITECTURES
Memory Architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers.

TOTAL : 45 PERIODS

COURSE OUTCOMES:
- To use mathematical methods and circuit analysis models in analysis of CMOS digital circuits
- To be able to create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort
- To design sequential logic at the transistor level and Compare the tradeoffs of sequencing elements including flip-flops, transparent latches
- To learn design methodology of arithmetic building blocks
- To design functional units including ROM and SRAM

REFERENCES:
OBJECTIVES:

• Analog circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology. The most important building blocks of all CMOS analog ICs will be the topic of study in this course.

• The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.

• The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.

UNIT I  SINGLE STAGE AMPLIFIERS

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower differential with active load, Cascode and folded cascode configurations with active load, Design of differential and cascode amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, High gain amplifier, structures.

UNIT II  HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS

Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III  FEEDBACK AND ONE STAGE OPERATIONAL AMPLIFIERS

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV  STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER

Analysis of two stage Op amp – two stage Op amp single stage CMOS Cs as second stage and using cascode second stage, multiple systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slew in two stage Op Amps, Other compensation techniques.
UNIT V  BANDGAP REFERENCES

Current sinks and sources, Current mirrors, Wilson current source, Wildar current source, Cascode current source, Design of high swing cascode sink, current amplifiers, Supply independent biasing, temperature independent references, PTAT and CTAT current generation, Constant-Gm Biasing.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to design amplifiers to meet user specifications
CO2: Ability to analyse the frequency and noise performance of amplifiers
CO3: Ability to design and analyse feedback amplifiers and one stage op amps
CO4: Ability to design and analyse two stage op amps
CO5: Ability to design and use current mirrors and current sinks with MOS devices

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OBJECTIVES:
- The course focuses on the semi-custom IC Design and introduces the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles.
- The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I  INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN
Types of ASICS - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.
UNIT II
PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND
PROGRAMMABLE ASIC I/O CELLS

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera
FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III
PROGRAMMABLE ASIC ARCHITECTURE

Architecture and configuration of Artix / Cyclone and Kintex Ultra Scale / Stratix FPGAs –
Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV
LOGIC SYNTHESIS, PLACEMENT AND ROUTING

Logic synthesis - Floor Planning Goals and Objectives, Measurement of Delay in floor planning,
Floor planning tools, I/O and Power planning, Clock planning, Placement Algorithms. Routing:
Global routing, Detailed routing, Special routing.

UNIT V
SYSTEM-ON-CHIP DESIGN

SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based
Communication Architectures, High performance filters using delta-sigma modulators.
Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to apply logical effort technique for predicting delay, delay minimization and FPGA
architectures
CO2: Ability to design logic cells and I/O cells
CO3: Ability to analyze the various resources of recent FPGAs
CO4: Ability to use algorithms for floor planning and placement of cells and to apply routing
algorithms for optimization of length and speed.
CO5: Ability to analyze high performance algorithms available for ASICs

REFERENCES:
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, "FPGA-based Implementation of
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc
7. S.Pasricha and N.Dutt, “On-Chip Communication Architectures System on Chip

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OBJECTIVES:
To impart knowledge and skills required for research and IPR:
- Problem formulation, analysis and solutions.
- Technical paper writing / presentation without violating professional ethics
- Patent drafting and filing patents.

UNIT I RESEARCH PROBLEM FORMULATION
Meaning of research problem- Sources of research problem, criteria characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations

UNIT II LITERATURE REVIEW
Effective literature studies approaches, analysis, plagiarism, and research ethics.

UNIT III TECHNICAL WRITING / PRESENTATION
Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal, a presentation and assessment by a review committee.

UNIT IV INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR)

UNIT V INTELLECTUAL PROPERTY RIGHTS (IPR)

TOTAL: 30 PERIODS

COURSE OUTCOMES:
CO1: Ability to formulate research problem
CO2: Ability to carry out research analysis
CO3: Ability to follow research ethics
CO4: Ability to understand that today’s world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity
CO5: Ability to understand about IPR and filing patents in R & D.
REFERENCES:

VL5161 ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY L T P C 0 0 4 2

OBJECTIVES:
- Students will carry out a detailed analog circuit design starting with transistor characterization and finally realizing an IA design.
- At various stages of design, a typical state of art CAD VLSI tool will be used in various phases of experiments designed to bring out the key aspects of each important module in the CAD tool including the simulation, layout, LVS and parasitic extracted simulation.

List of Experiments:
1. Extraction of process parameters of CMOS process transistors
   a. Plot \( I_D \) vs. \( V_{GS} \) at different drain voltages for NMOS, PMOS.
   b. Plot \( I_D \) vs. \( V_{GS} \) at particular drain voltage (low) for NMOS, PMOS and determine \( V_t \).
   c. Plot \( \log I_D \) vs. \( V_{GS} \) at particular gate voltage (high) for NMOS, PMOS and determine \( I_{OFF} \) and sub-threshold slope.
   d. Plot \( I_D \) vs. \( V_{DS} \) at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e. Extract \( V_{th} \) of NMOS/PMOS transistors (short channel and long channel). Use \( V_{DS} \) of appropriate voltage To extract \( V_{th} \) use the following procedure.
      i. Plot \( g_m \) vs \( V_{GS} \) using SPICE and obtain peak \( g_m \) point.
      ii. Plot \( y=I_D/(g_m) \) as a function of \( V_{GS} \) using SPICE.
      iii. Use SPICE to plot tangent line passing through peak \( g_m \) point in \( y(V_{GS}) \) plane and determine \( V_{th} \).
   f. Plot \( I_D \) vs. \( V_{DS} \) at different drain voltages for NMOS, PMOS, plot DC load line and calculate \( g_m, g_{ds}, g_{m/gds} \), and unity gain frequency. Tabulate result according to technologies and comment on it.

2. CMOS inverter design and performance analysis
   a. Plot VTC curve for CMOS inverter and thereon plot \( dV_{out} \) vs. \( dV_{in} \) and determine transition voltage and gain \( g \). Calculate \( V_{IL}, V_{IH}, N_{MH}, N_{ML} \) for the inverter.
      i. Plot VTC for CMOS inverter with varying \( V_{DD} \).
      ii. Plot VTC for CMOS inverter with varying device ratio.
   b. Perform transient analysis of CMOS inverter with no load and with load and determine \( t_{pHL}, t_{pLH}, 20\%\text{-to-}80\% \) and \( 80\%\text{-to-}20\% \).
   c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.

4. Single stage amplifier design and performance analysis
   a. Draw small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.
   b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
      i. Establish a test bench to achieve \( V_{DSQ}=V_{DD}/2 \).
      ii. Calculate input bias voltage for a given bias current.
      iii. Use spice and obtain the bias current. Compare with the theoretical value
      iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier
using small signal analysis in spice, considering load capacitance.

v. Plot step response of the amplifier with a specific input pulse amplitude. Derive time constant of the output and compare it with the time constant resulted from -3dB BW.

vi. Use spice to determine input voltage range of the amplifier

5. Three OPAMP Instrumentation Amplifier.

Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

i. Draw the schematic of op-amp macro model.

ii. Draw the schematic of INA.

iii. Obtain parameters of the op-amp macro model such that it meets a given specification for:

   i. low-frequency voltage gain,
   ii. unity gain BW (fu),
   iii. input capacitance,
   iv. output resistance,
   v. CMRR

iv. Draw schematic diagram of CMRR simulation setup.

ev. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

vii. Repeat (i) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6. Use Layout editor.

a. Draw layout of a minimum size inverter using transistor from CMOS process library. Use Metal 1 as interconnect line between inverters.

b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.

c. Extract the netlist. Use extracted netlist and obtain $t_{PHL}$ $t_{PLH}$ for the inverter using Spice.

d. Use a specific interconnect length and connect and connect three inverters in a chain. Extract the new netlist and obtain $t_{PHL}$ and $t_{PLH}$ of the middle inverter.

e. Compare new values of delay times with corresponding values obtained in part 'c'.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter:

   a. low-frequency voltage gain,
   b. unity gain BW (fu),
   c. Power dissipation

   i. Perform DC analysis and determine input common mode range and compare with the theoretical values.
   ii. Perform time domain simulation and verify low frequency gain.
   iii. Perform AC analysis and verify.

TOTAL: 60 PERIODS

COURSE OUTCOMES:

CO1: Design digital and analog Circuit using CMOS given a design specification.

CO2: Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances

CO3: Use EDA tools like Cadence, Mentor Graphics or other open source software tools like LTSpice

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OBJECTIVES
- To impart hands on experience in single, double and multi layer PCB design so that students would be able to design and to fabricate and develop electronic systems for various applications.

LIST OF EXPERIMENTS:
1. Introduction to PCB and EDA software tools.
2. To prepare design layout of PCBs using software tools.
3. To fabricate simple PCB by chemical and mechanical process and drilling of PCB.
4. To fabricate PCB using additive technology and testing of electronics circuit on PCB.
5. To perform Assembly Processes - Manual assembly processes,
6. To perform automated assembly processes (pick and place).
7. Identification of various types of Printed Circuit Boards (PCB) and soldering Techniques.
8. Convert the power supply circuit into PCB and simulate its 2D and 3D view.
9. Design and create single sided PCB Layout for Full wave rectifier circuit.
10. Design and create PCB Layout for DC Motor controller.
11. Design and create single sided PCB Layout for Flashing LEDs using 555 IC.
12. LED Scrolling Display Board using microcontroller
13. To perform continuity tester of PCB project.
14. To implement a Digital Counter To fabricate the PCB for the same.
15. To fabricate PCB dual power supply, analog design.
16. To fabricate PCB with Split power and ground planes.

TOTAL : 60 PERIODS

COURSE OUTCOMES:
CO1: Ability to use CAD software tools
CO2: Ability to design a schematic diagram
CO3: Ability to convert a schematic diagram to board/layout diagram
CO4: Implement routing in board/layout diagram
CO5: Ability to fabricate a PCB from board diagram
CO6: Ability to skillfully perform assembling and soldering of components

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OBJECTIVES:
- To expose the students to the fundamentals of embedded system design.
- To enable the students to understand and use embedded computing platform.
- To introduce networking principles in embedded devices.
- To learn real time characteristics in embedded system design.
- To explore system design techniques.
UNIT I  EMBEDDED PROCESSORS  9

UNIT II  EMBEDDED COMPUTING PLATFORM  9
Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example: Alarm Clock.

UNIT III  NETWORKS  9
Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV  REAL-TIME CHARACTERISTICS  9

UNIT V  SYSTEM DESIGN TECHNIQUES  9

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: To explore fundamentals of embedded system design.
CO2: To interpret and use embedded computing platform.
CO3: To apply networking principles in embedded devices.
CO4: To gain insight on the characteristics in embedded system design.
CO5: To select and design suitable embedded systems for real world applications.

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OBJECTIVES:
- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent methods.
- Identify suitable techniques to reduce the power dissipation.
- Estimate Power dissipation of various MOS logic circuits.
- Develop algorithms for low power dissipation.

UNIT I  POWER DISSIPATION IN CMOS
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II  POWER OPTIMIZATION
Logic level power optimization – Circuit level low power design – Gate level low power design – Architecture level low power design – VLSI subsystem design of adders, multipliers, PLL, low power design.

UNIT III  DESIGN OF LOW POWER CMOS CIRCUITS
Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – Advanced techniques – Special techniques, Adiabatic techniques – Physical design, Floor planning, placement and routing.

UNIT IV  POWER ESTIMATION
Power Estimation techniques, circuit level, gate level, architecture level, behavioral level, – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V  SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER
Synthesis for low power – Behavioral level transform –Algorithms for low power – software design for low power.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to find the power dissipation of MOS circuits
CO2: Design and analyse various MOS logic circuits
CO3: Apply low power techniques for low power dissipation
CO4: Able to estimate the power dissipation of ICs
CO5: Ability to develop algorithm to reduce power dissipation by software.

REFERENCES:
AP5153 STATISTICAL SIGNAL PROCESSING L T P C 3 0 0 3

OBJECTIVES:
- To introduce the basics of random signal processing
- To learn the concept of estimation and prediction theory
- To know about adaptive filtering and its applications

UNIT I INTRODUCTION TO RANDOM SIGNAL PROCESSING 9

UNIT II SIGNAL MODELING 9
ARMA (p,q) , AR (p), MA (q) models, Forward Linear Prediction, Backward Linear Prediction: – Yule-Walker Method, Solution to Prony’s normal equation, Levinson Durbin Algorithm.

UNIT III SPECTRAL ESTIMATION 9
Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric method, AR (p) spectral estimation and detection of Harmonic signals.

UNIT IV LINEAR ESTIMATION 9

UNIT V ADAPTIVE FILTERS 9

TOTAL : 45 PERIODS

COURSE OUTCOMES:
CO1: Analyze discrete time random processes
CO2: Obtain models for prediction and Estimation
CO3: Analyze non-parametric methods and parametric methods for spectral estimation
CO4: Design different MMSE filters
CO5: Design adaptive filters for different applications
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AP5161 EMBEDDED SYSTEMS AND ROBOTICS LABORATORY

OBJECTIVES:
- To introduce microcontroller based system design concept.
- To learn concept on real time operating systems.
- To make learn EDA tools, sensors, high power devices and motors.
- To work with different Robots and its operating systems.

EMBEDDED SYSTEMS LAB EXPERIMENTS:
1. Microcontroller based system design of interfacing with RTC, LCD and I2C EPROM.
2. Design of microcontroller based RC5 remote control decoder.
3. Microcontroller based system design of Switching of high power device with SCR, MOSFET and Relay.
4. Microcontroller based system design with Touch screen interfacing.
5. Sensors and interfacing of ultrasound sensors, PIR, temperature and RFID with Microcontroller based system.
6. Microcontroller based system design with Matrix keyboard and LED interfacing.
7. Microcontroller based system design with Motor interfacing-DC, servo and stepper.
8. Design and implementation of different real time scheduling algorithms for embedded applications. RTOS- simple task creation, Round Robin Scheduling and Semaphores.

ROBOTICS LAB EXPERIMENTS:
1. Design and implementation of Line following Robot.
2. Design and implementation of Obstacle avoidance and navigation Robot.
3. Design and implementation of Robotic Arm manipulation with 6 DOF.
4. Design and implementation of Pick and Place robot.
5. Design and implementation of Colour guided material handling Robot.
6. Design and implementation of Self balancing robot.
7. Robot operating System (ROS) for Robot.

**COURSE OUTCOMES:**
CO1: Ability to design and develop microcontroller based systems.
CO2: Validate the design in microcontroller starting from assembler to compiler.
CO3: Ability to use EDA tools, sensors, high power devices and motors.
CO4: Ability to design and develop different real-time scheduling algorithms.
CO5: Ability to work with different Robot operating systems.

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**TOTAL: 60 PERIODS**

**VL5261 SIGNAL PROCESSING AND RTL SYNTHESIS LABORATORY**

**OBJECTIVES:**
- FPGAs are important platform used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes, the students will be carrying out complete hardware level FPGA validation of important digital algorithms.
- Understanding signal processing play a key role in the design and testing of circuit block in ICs. The experiments are structured to give an exposure to the design of basic signal processing modules and its realization in FPGA

**LIST OF EXPERIMENTS:**
1) HDL realization and timing analysis of
   i. Combinational circuits namely 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder.
   ii. Sequential circuits namely D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters.
2) FPGA implementation of PCI Bus & arbiter.
3) Realization of UART/ USART implementation in HDL and design validation using test vector generation.
4) FPGA realization of single port SRAM and capturing the signal in DSO.
5) Back annotation and timing analysis of Arithmetic circuits like serial adder/subtractor, parallel adder/subtractor, serial/parallel multiplier.
6) Realization of Discrete Fourier transform/Fast Fourier Transform algorithm in HDL and observing the spectrum in simulation.
7) Implement different power spectrum
8) Design and implement FIR and IIR Weiner filters for smoothing and prediction
9) Design and implement adaptive filters
10) Perform image enhancement operations (spatial & transform domain analysis)
11) Perform morphological image analysis
12) Implement image segmentation algorithms

TOTAL : 60 PERIODS

COURSE OUTCOMES:

CO1: Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
CO2: Validate the design in FPGA starting from design entry to back annotation.
CO4: Implement image processing algorithms using MATLAB and HDL
CO5: Implement image processing algorithms using MATLAB and HDL

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AP5078 WIRELESS SENSOR NETWORKS L T P C
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OBJECTIVES:

- To enable the student to understand the role of sensors and the networking of sensed data for different applications.
- To expose the students to the sensor node essentials and the architectural details, the medium access and routing issues and the energy constrained operational scenario.
- To enable the student to understand the challenges in synchronization and localization of sensor nodes, topology management for effective and sustained communication, data management and security aspects

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9

UNIT II ARCHITECTURES 9

UNIT III MAC AND ROUTING 9
UNIT IV   INFRASTRUCTURE ESTABLISHMENT  
Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT V   DATA MANAGEMENT AND SECURITY  
Data management in WSN, Storage and indexing in sensor networks, Query processing in sensor, Data aggregation, Directed diffusion, Tiny aggregation, greedy aggregation, security in WSN.

TOTAL : 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to design implement simple wireless network concepts
CO2: Ability to design, analyze implement different network architectures
CO3: Ability to implement MAC layer and routing protocols
CO4: Ability to deal with timing and control issues in wireless sensor networks
CO5: Ability to analyze and design secured wireless sensor networks

REFERENCES
OBJECTIVES:

- To expose the students to the basics of PCB design
- To lead the new users of the software through a very simple design
- To address the mechanical aspect of PCB design and to aid in understanding the design issues, manufacturing processes.
- To address the electrical aspect of PCB design
- To expose the students to the state of art technology in PCB design and manufacturing

UNIT I  BASICS OF PCB DESIGN, TOOLS & INDUSTRY STANDARDS  9
Printed Circuit Board Fabrication- PCB cores and layer stack-up. PCB fabrication process- Photolithography and chemical etching, Mechanical Layer registration. Function of the Layout in the PCB Design Process. Design Files Created by Layout - Layout format files, Postprocess (Gerber) files, PCB assembly layers and files. Introduction to the Standards Organizations, Classes and Types of PCBs, Introduction to Standard Fabrication Allowances, PCB Dimensions and Tolerances, Copper Trace and Etching Tolerances, Standard Hole Dimensions, Soldermask Tolerance.

UNIT II  PCB DESIGN FLOW USING CAD TOOL  9
Overview of Computer-Aided Design. Project structures and the layout toolset- Project Setup and Schematic Entry Details, the Layout Environment and Tool Set. Creating a Circuit Design with Capture-Starting a new project placing parts, Wiring (connecting) the parts, creating the Layout netlist in Capture. Designing the PCB with Layout- Starting Layout and importing the netlist, Performing a design rule check, Making a board outline, Placing the parts, Auto routing the board Manual routing, Cleanup Locking traces, Post processing the board design for manufacturing. Setting up a user account, Submitting Gerber files and requesting a quote, Annotating the layer types and stack-up, Receipt inspection and testing, Nonstandard Gerber files.

UNIT III  DESIGN FOR MANUFACTURING  9

UNIT IV  PCB DESIGN FOR SIGNAL INTEGRITY  9

UNIT V  EMERGING ADDITIVE PROCESSES FOR PCB MANUFACTURING  9

TOTAL : 45 PERIODS
COURSE OUTCOMES
CO1: To understand the basics, industry standards organizations related to the design and fabrication of PCBs.
CO2: Leads new users of the software through a very simple design
CO3: To know and guide in designing plated through-holes, surface-mount lands, and Layout footprints in general.
CO4: To know to construct Capture parts using the Capture Library Manager and Part Editor and the PSpice Model Editor.
CO5: To understand and to fabricate PCBs

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AP5071 ADVANCED MICROPROCESSORS & MICROCONTROLLERS L T P C 3 0 0 3

OBJECTIVES:
- To expose the students to the fundamentals of microprocessor architecture.
- To explore the high performance features in CISC architecture
- To familiarize the high performance features in RISC architecture
- To introduce the basic features in Motorola microcontrollers.
- To enable the students to understand PIC Microcontroller

UNIT I MICROPROCESSOR ARCHITECTURE

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM
UNIT III  HIGH PERFORMANCE RISC ARCHITECTURE – ARM  9
Organization of CPU – Bus architecture – Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV  MSP430 16 - BIT MICROCONTROLLER  9

UNIT V  PIC MICROCONTROLLER  9

TOTAL:45 PERIODS

COURSE OUTCOMES:
CO1: To understand the fundamentals of microprocessor architecture.
CO2: To know and appreciate the high performance features in CISC architecture.
CO3: To know and appreciate the high performance features in RISC architecture.
CO4: To perceive the basic features in Motorola microcontrollers.
CO5: To interpret and understand PIC Microcontroller.

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OBJECTIVES

- Study the behavior of photovoltaic solar energy systems, focusing on the behavior of “stand-alone” systems.
- Do a first order, conceptual design of a stand-alone system for a location anywhere in India.
- Introduce the hardware elements and their behavior.
- Select battery for a PV system and battery sizing.
- Simulate standalone and grid tied PV system.

UNIT I  INTRODUCTION TO SOLAR POWER
Semiconductor – properties - energy levels - basic equations of semiconductor devices physics - Basic characteristics of sunlight - Solar angles - day length - angle of incidence on tilted surface – Sun path diagrams – Equivalent circuit of PV cell, PV cell characteristics (VI curve, PV curve) - Maximum power point, Vmp, Imp, Voc, Isc – types of PV cell - Block diagram of solar photo voltaic system, PV array sizing.

UNIT II  DC-DC CONVERTER

UNIT III  MAXIMUM POWER POINT TRACKING

UNIT IV  BATTERY
Types of Battery, Battery Capacity – Units of Battery Capacity-impact of charging and discharging rate on battery capacity-Columbic efficiency-Voltage Efficiency, Charging – Charge Efficiency, Charging methods, State of Charge, Charging Rates, Discharging - Depth of discharge-Discharge Methods, Circuits for Battery Management System (BMS), selection of Battery and sizing.

UNIT V  SIMULATION OF PV MODULE & CONVERTERS
Simulation of PV module - VI Plot, PV Plot, finding Vmp, Imp, Voc, Isc of PV module, Simulation of DC to DC converter -buck, boost, buck-boost and Cuk converters, standalone and grid tied photo voltaic system.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to collect solar power characteristics at a given location
CO2: Ability to design and realize dc-dc converters for solar power utilization
CO3: Ability to design algorithms for improving solar power utilization
CO4: Ability to deal with battery issues and selection
CO5: Ability to design and simulate PV systems to validate its performance.

REFERENCES:
OBJECTIVES:
- To Teach the basic concepts in robotics.
- To expose the various design aspects in robot grippers.
- To make learn various drives and control systems.
- To impart knowledge on machine vision systems.
- To apply robot based concepts for automation

UNIT I INTRODUCTION:
Basic Concepts such as Definition, three laws, DOF, Misunderstood devices etc., Elements of Robotic Systems i.e. Robot anatomy, Classification, Associated parameters i.e. resolution, accuracy, repeatability, dexterity, compliance, RCC device, etc. Automation-Concept, Need, Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations, introduction to automation productivity.

UNIT II ROBOT GRIPPERS:
Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system. Sensors for Robots:- Characteristics of sensing devices, Selections of sensors, Classification and applications of sensors. Types of Sensors, Need for sensors and vision system in the working and control of a robot.

UNIT III DRIVES AND CONTROL SYSTEMS:

UNIT IV MACHINE VISION SYSTEM
Vision System Devices, Robot Programming:- Methods of robot programming, lead through programming, motion interpolation, branching capabilities, WAIT, SIGNAL and DELAY commands, subroutines, Programming Languages: Introduction to various types such as RAIL and VAL II etc, Features of type and development of languages for recent robot systems.
UNIT V  MODELING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION


COURSE OUTCOMES:
- Ability to implement simple concepts associated with Robotics and Automation
- Ability to use various Robotic sub-systems
- Ability to use kinematics and dynamics to design exact working pattern of robots
- Ability to implement computer vision algorithms for robots
- Be aware of the associated recent updates in Robotics

REFERENCES:

AP5075  RF SYSTEM DESIGN

OBJECTIVES:
- The students will learn various design steps starting from system specifications to hardware/software implementation and will experience process optimization while considering various design decisions.
- Students will gain design experience with project/case studies using contemporary high-level methods and tools.

UNIT I  CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter.

UNIT II  IMPEDANCE MATCHING AND AMPLIFIERS

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.
UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS
Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT IV MIXERS AND OSCILLATORS
Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS
Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to collect user specifications for RF systems
CO2: Ability to analyze and design RF amplifiers
CO3: Ability to analyze and design RF power amplifiers
CO4: Ability to analyze and design RF mixers and oscillators
CO5: Ability to design PLL for RF applications

REFERENCES:
5. Recorded lectures and notes available at . http://www.ee.iitm.ac.in/~ani/ee6240/

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AP5077 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN

OBJECTIVES:
- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES
Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance, wave propagation, reflection, and bounce diagrams Reactive terminations – L, C, static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching, input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.
UNIT II  MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK  9
Multi-conductor transmission-lines, coupling physics, per unit length parameters, near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits, S-parameters, Lossy and Lossless models.

UNIT III  NON-IDEAL EFFECTS  9
Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses – Rs, tanδ, routing parasitic, Common-mode current, differential-mode current, Connectors.

UNIT IV  POWER CONSIDERATIONS AND SYSTEM DESIGN  9
SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis.

UNIT V  CLOCK DISTRIBUTION AND CLOCK OSCILLATORS  9
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL : 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to identify sources affecting the speed of digital circuits.
CO2: Ability to identify methods to improve the signal transmission characteristics

REFERENCES

TOOLS REQUIRED
1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html

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OBJECTIVES:
- To understand the concepts related to Electromagnetic interference in PCBs.
- To provide solutions for minimizing EMI in PCBs.
- To learn various EMI coupling principles.
- To indulge knowledge on EMI control techniques and design procedures to make EMI compatible PCBs.
- To learn electromagnetic compatibility issues with regard to the design of PCBs.
- To learn, EMI standards and measurements in the design of PCBs.

UNIT I   EMI/EMC CONCEPTS
EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II   EMI COUPLING PRINCIPLES
Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling; Cross talk; Field to cable coupling; Power mains and Power supply coupling.

UNIT III   EMI CONTROL TECHNIQUES
Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV   EMC DESIGN OF PCBs
Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V   EMI MEASUREMENTS AND STANDARDS
Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Gain enough knowledge to understand the concept of EMI / EMC related to product design & development.
CO2: To analyze the different EM coupling principles and its impact on performance of electronic system.
CO3: Analyze electromagnetic interference, highlighting the concepts of both susceptibility and immunity.
CO4: Interpret various EM compatibility issues with regard to the design of PCBs and ways to improve the overall system performance.
CO5: To obtain broad knowledge of various EM radiation measurement techniques and the present leading edge industry standards in different countries.

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VL5001 HARDWARE SOFTWARE CO-DESIGN

OBJECTIVES:
- To acquire the knowledge about system specification and modelling
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation

UNIT I SYSTEM SPECIFICATION AND MODELLING

UNIT II HARDWARE/SOFTWARE PARTITIONING
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV PROTOTYPING AND EMULATION

UNIT V DESIGN SPECIFICATION AND VERIFICATION

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Describe the broad range of system architectures and design methodologies that currently exist and define their fundamental attributes.
CO2: Discuss the dataflow models as a state-of-the-art methodology to solve co-design problems and to optimize the balance between software and hardware.
CO3: Understand in translating between software and hardware descriptions through co-design methodologies.
CO4: Understand the state-of-the-art practices in developing co-design solutions to problems using modern hardware/software tools for building prototypes.
CO5: Understand the concurrent specification from an algorithm, analyze its behavior and partition the specification into software (C code) and hardware (HDL) components.
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VL5002 RECONFIGURABLE COMPUTING L T P C
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OBJECTIVES:
- To study about the reconfigurable computing architectures
- Understand the concepts of software flexibility and hardware performance
- Usage of high speed computing fabrics like field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs)
- Design and applications of dynamic and partial reconfigurable computing systems

UNIT I RECONFIGURABLE COMPUTING HARDWARE 9

UNIT II PROGRAMMING RECONFIGURABLE SYSTEMS 9

UNIT III MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS 9
Technology Mapping, Placement for General-purpose FPGAs, Datapath Composition, Specifying Circuit Layout on FPGAs, PathFinder: A Negotiation-based, Performance-driven Router for FPGAs, Retiming, Repipelining, and C-slow Retiming, Configuration Bitstream Generation, Fast Compilation Techniques
UNIT IV APPLICATION DEVELOPMENT
Implementing Applications with FPGAs, Instance-specific Design, Precision Analysis for Fixed-point Computation, Distributed Arithmetic, CORDIC Architectures for FPGA Computing, Hardware/Software Partitioning

UNIT V CASE STUDIES OF FPGA APPLICATIONS
SPIHT ImageCompression, Automatic Target Recognition Systems on Reconfigurable Devices, Multi-FPGA Systems: Logic Emulation, The Implications of Floating Point for FPGAs, Evolvable FPGAs, Network Packet Processing in Reconfigurable Hardware, Active Pages: Memory-centric Computation

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Understand the fundamentals of the reconfigurable computing and reconfigurable architectures.
CO2: Articulate the design issues involved in reconfigurable computing systems with a specific focus on Field Programmable Gate Arrays (FPGAs) both in theoretical and application levels.
CO3: Understand the performance trade-offs involved in designing a reconfigurable computing platform with a specific focus on the architecture of a configurable logic block and the programmable interconnect.
CO4: Discuss the state of the art reconfigurable computing architectures spanning fine grained (look up table based processing elements) to coarse grained (arithmetic logic unit level processing elements) architectures.
CO5: Understand both how to architect reconfigurable systems and how to utilize them for solving challenging computational problems.

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VL5003 EVOLVABLE HARDWARE  L  T  P  C
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OBJECTIVES:
- To study about the Evolvable Systems algorithms, multi-objective utility functions
- Understand the concepts of reliability, design-in redundancy, fault tolerance and defect tolerance
- Design of evolvable systems using programmable logic devices (like FPGAs) and modular subsystems with identical components and generalized controller algorithms
UNIT I  INTRODUCTION  9
Traditional hardware systems and its Limitations, Evolvable hardware, Characteristics of
evolvable circuits and systems, Technology-Extrinsic and intrinsic evolution Offline and online
evolution, Applications and scope of EHW

UNIT II  EVOLUTIONARY COMPUTATION  9
Fundamentals of Evolutionary algorithms, Components of EA, Variants of EA, Genetic
algorithms, Genetic Programming, Evolutionary strategies, Evolutionary programming,
Implementations – Evolutionary design and optimizations, EHW – Current problems and
potential solutions

UNIT III  RECONFIGURABLE DIGITAL DEVICES  9
Basic architectures – Programmable Logic Devices, Field Programmable Gate Arrays (FPGAs),
Using reconfigurable hardware – Design phase, Execution phase, Evolution of digital circuits

UNIT IV  RECONFIGURABLE ANALOG DEVICES  9
Basic architectures – Field Programmable Transistor arrays (FPTAs), Analog arrays, MWMs,
Using reconfigurable hardware – Design phase, Execution phase, Evolution of analog circuits

UNIT V  APPLICATIONS OF EHW  9
Synthesis vs. adaptation, Designing self-adaptive systems, Fault-tolerant systems, Real-time
systems, intrinsic reconfiguration for online systems, EHW based fault recovery and future work

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Understand the fundamentals of computational models and computers which have
appeared at the intersection of hardware and artificial intelligence to solve hard
computational problems.
CO2: Understand the principles of bio-inspired and unconventional computational systems.
CO3: Discuss about the reconfigurable digital architectures and its computational intelligence
techniques.
CO4: Discuss about the reconfigurable analog architectures and its computational intelligence
techniques.
CO5: Discuss about the typical applications of bio-inspired and other unconventional
techniques in the phase of design, implementation and runtime of a computational
device.

REFERENCES:
1. Garrison W. Greenwood and Andrew M. Tyhrrell, “Introduction to Evolvable Hardware: A
3. Lukas Sekanina, “Evolvable Components: From Theory to Hardware Implementations”,
OBJECTIVES:
- To teach the design of reference circuits and low drop out regulators for desired specifications
- To teach oscillator choice and requirements for clock generation circuits
- To teach the design of clock generation and recovery in the context of high speed systems

UNIT I VOLTAGE AND CURRENT REFERENCES
Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference, Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II LOW DROP OUT REGULATORS

UNIT III OSCILLATOR FUNDAMENTALS
General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for LC & Ring Oscillators, Phase Noise in Differential LC Oscillators.

UNIT IV CLOCK DISTRIBUTION CIRCUITS

UNIT V CLOCK AND DATA RECOVERY CIRCUITS
CDR Architectures, Trans Impedance Amplifiers and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Design Band gap reference circuits and Low Drop Out regulator for a given specification.
CO2: Understand specification related to Supply and Clock generation circuits of ICs
CO3: Choose oscillator topology and design meeting the requirement of clock generation circuits.
CO4: Design clock generation circuits in the context of high speed I/Os, High speed Broad Band Communication circuits and Data Conversion Circuits.
CO5: Band Communication circuits and Data Conversion Circuits.

REFERENCES:
OBJECTIVES:
- To introduce the VLSI Testing.
- To introduce Logic and Fault Simulation and Testability Measures.
- To study the Test Generation for Combinational and Sequential Circuits,
- To study the Design for Testability.
- To study the Fault Diagnosis

UNIT I  INTRODUCTION TO TESTING  9

UNIT II  LOGIC &FAULT SIMULATION & TESTABILITY MEASURES  9

UNIT III  TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS  9

UNIT IV  DESIGN FOR TESTABILITY  9

UNIT V  FAULT DIAGNOSIS  9
Introduction and Basic Definitions – Fault Models for Diagnosis – Generation for Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO2: Develop Logic Simulation and Fault Simulation.
CO3: Develop Test for Combinational and Sequential Circuits.
CO4: Understand the Design for Testability.
CO5: Perform Fault Diagnosis.

REFERENCES:
OBJECTIVES:
- To understand the formulation of SoC based designs
- To teach SoC based design approaches
- To teach low power SoC design approaches

UNIT I  ASIC
Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC, architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT II  NISC
NISC Control Words methodology, NISC Applications & Advantages, Architecture, Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC) - design flow, modelling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT III  SIMULATION
Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT IV  LOW POWER SOC DESIGN / DIGITAL SYSTEM
- Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT V  SYNTHESIS
- Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis, Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Identify & formulate a given problem in framework of SoC based design approaches
CO2: Design SoC based system for engineering applications
CO3: Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.
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VL5007 DATA CONVERTERS

OBJECTIVES:
- To teach A to D and D to A characteristics
- To teach the design of switched capacitor based circuits
- To teach the design of A/D and D/A converters

UNIT I INTRODUCTION & CHARACTERISTICS OF AD/DA CONVERTER CHARACTERISTICS
Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and antialiasing filters.

UNIT II SWITCH CAPACITOR CIRCUITS AND COMPARATORS
Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques

UNIT III NYQUIST RATE D/A CONVERTERS
Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues in current element matching, clock feed through, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs

UNIT IV PIPELINE AND OTHER ADCs
Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V SIGMA DELTA CONVERTERS
STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Opamp nonlinearities

TOTAL : 45 PERIODS
COURSE OUTCOMES:
CO1: Ability to carry out the design calculations for developing the various blocks associated with a typical CMOS AD or DA converter.
CO2: Ability to design and implement circuits using switched capacitor concepts
CO3: Ability to analyze and design D/A converters
CO4: Ability to design different types of A/Ds
CO5: Ability to analyze and design sigma delta converters

REFERENCES:
6. VLSI Data Conversion Circuits EE658 recorded lectures available at http://www.ee.iitm.ac.in/~nagendra/videolecture

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VL5008 CAD FOR VLSI CIRCUITS

OBJECTIVES:
- To introduce the VLSI Design Methodologies and Design Methods.
- To introduce Data Structures and Algorithms required for VLSI Design.
- To study Algorithms for Partitioning and Placement.
- To study Algorithms for Floor planning and Routing.
- To study Algorithms for Modelling, Simulation and Synthesis.

UNIT I INTRODUCTION

UNIT II DATA STRUCTURES AND BASIC ALGORITHMS

UNIT III ALGORITHMS FOR PARTITIONING AND PLACEMENT
UNIT IV  ALGORITHMS FOR FLOORPLANNING AND ROUTING  9
Floorplanning – Problem Formulation – Floorplanning Algorithms – Routing – Area Routing –
Global Routing – Detailed Routing.

UNIT V  MODELLING, SIMULATION AND SYNTHESIS  9
Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary
Decision Diagrams – High Level Synthesis.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Use various VLSI Design Methodologies and Design Methods.
CO2: Understand different Data Structures and Algorithms required for VLSI Design.
CO3: Develop Algorithms for Partitioning and Placement.
CO4: Develop Algorithms for Floorplanning and Routing.
CO5: Design Algorithms for Modelling, Simulation and Synthesis.

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VL5009  VLSI SIGNAL PROCESSING  L T P C  3 0 0 3

OBJECTIVES:
- To introduce techniques for altering existing DSP structures to suit
  VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I  INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL
          PROCESSING OF FIR FILTERS  9
Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence
graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm,
Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for
low power.

UNIT II  RETIMING, ALGORITHMIC STRENGTH REDUCTION  9
Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties
of unfolding, sample period reduction and parallel processing application, Algorithmic
strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter,
DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-
order filters.
UNIT III  FAST CONVOLUTION, PIPELINING AND PARALLEL  
PROCESSING OF IIR FILTERS  
Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and  
parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead  
pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel  
processing of IIR filters, combined pipelining and parallel processing of IIR filters.  

UNIT IV  BIT-LEVEL ARITHMETIC ARCHITECTURES  
Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-  
ripple and carry-save multipliers, Design of Lyon’s bit-serial multipliers using Horner’s  
rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for  
precision improvement, Distributed Arithmetic fundamentals and FIR filters  

UNIT V  NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS,  
WAVE AND ASYNCHRONOUS PIPELINING  
Numerical strength reduction – sub expression elimination, multiple constant  
multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew  
in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous  
pipelining bundled data versus dual rail protocol.  

COURSE OUTCOMES:  
CO1: Ability to determine the parameters influencing the efficiency of DSP architectures and  
apply pipelining and parallel processing techniques to alter FIR structures for  
efficiency  
CO2: Ability to analyse and modify the design equations leading to efficient DSP  
architectures for transforms  
CO3: Ability to speed up convolution process and develop fast and area efficient IIR  
structures  
CO4: Ability to develop fast and area efficient multiplier architectures  
CO5: Ability to reduce multiplications and build fast hardware for synchronous digital  
systems  

REFERENCES  
2. U. Meyer – Baese, “Digital Signal Processing with Field Programmable Gate  

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OBJECTIVES:

- To introduce methods to analyse and design synchronous sequential circuits
- To introduce methods to analyse and design asynchronous sequential circuits and to analyse hazards
- To introduce the fault testing procedure for combinational circuits and PLA circuits
- To introduce the architectures of programmable devices
- To introduce design and implementation of digital circuits using programming tools

UNIT I  SEQUENTIAL CIRCUIT DESIGN 9
Analysis of clocked synchronous sequential circuits and modelling - State diagram, state table, state table assignment and reduction - Design of synchronous sequential circuits design of iterative circuits - ASM chart and realization using ASM

UNIT II  ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9
Analysis of asynchronous sequential circuit - Flow table reduction - races - state assignment - transition table and problems in transition table - design of asynchronous sequential circuit - Static, dynamic and essential hazards - mixed operating mode asynchronous circuits - designing vending machine controller

UNIT III  FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9
Fault table method - path sensitization method - Boolean difference method - D algorithm - Kohavi algorithm - Tolerance techniques - The compact algorithm - Fault in PLA - Test generation-DFT schemes - Built in self test

UNIT IV  SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9
Programming logic device families - Designing a synchronous sequential circuit using PLA/PAL - Designing ROM with PLA - Realization of finite state machine using PLD - FPGA - Xilinx FPGA-Xilinx 4000

UNIT V  SYSTEM DESIGN USING VERILOG 9

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Analyse and design synchronous sequential circuits
CO2: Analyse hazards and design asynchronous sequential circuits
CO3: Knowledge on the testing procedure for combinational circuit and PLA
CO4: Able to design PLD and ROM
CO5: Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
OBJECTIVES:
- To understand the basics of business analytics and its life cycle.
- To gain knowledge about fundamental business analytics.
- To learn modeling for uncertainty and statistical inference.
- To understand analytics using Hadoop and Map Reduce frameworks.
- To acquire insight on other analytical frameworks.

UNIT I  OVERVIEW OF BUSINESS ANALYTICS

Suggested Activities:
- Case studies on applications involving business analytics.
- Converting real time decision making problems into hypothesis.
- Group discussion on entrepreneurial opportunities in Business Analytics.

Suggested Evaluation Methods:
- Assignment on business scenario and business analytical life cycle process.
- Group presentation on big data applications with societal need.
- Quiz on case studies.

UNIT II  ESSENTIALS OF BUSINESS ANALYTICS

Suggested Activities:
- Solve numerical problems on basic statistics.
- Explore chart wizard in MS Excel Case using sample real time data for data visualization.
- Use R tool for data visualization.
Suggested Evaluation Methods:
- Assignment on descriptive analytics using benchmark data.
- Quiz on data visualization for univariate, bivariate data.

UNIT III  MODELING UNCERTAINTY AND STATISTICAL INFERENCE  9

Suggested Activities:
- Solving numerical problems in sampling, probability, probability distributions and hypothesis testing.
- Converting real time decision making problems into hypothesis.

Suggested Evaluation Methods:
- Assignments on hypothesis testing.
- Group presentation on real time applications involving data sampling and hypothesis testing.
- Quizzes on topics like sampling and probability.

UNIT IV  ANALYTICS USING HADOOP AND MAPREDUCE FRAMEWORK  9

Suggested Activities:
- Practical – Install and configure Hadoop.
- Practical – Use web based tools to monitor Hadoop setup.
- Practical – Design and develop MapReduce tasks for word count, searching involving text corpus etc.

Suggested Evaluation Methods:
- Evaluation of the practical implementations.
- Quizzes on topics like HDFS and extensions to MapReduce.

UNIT V  OTHER DATA ANALYTICAL FRAMEWORKS  9
Overview of Application development Languages for Hadoop – PigLatin – Hive – Hive Query Language (HQL) – Introduction to Pentaho, JAQL – Introduction to Apache: Sqoop, Drill and Spark, Cloudera Impala – Introduction to NoSQL Databases – Hbase and MongoDB.

Suggested Activities:
- Practical – Installation of NoSQL database like MongoDB.
- Practical – Demonstration on Sharding in MongoDB.
- Practical – Install and run Pig
- Practical – Write PigLatin scripts to sort, group, join, project, and filter data.
- Design and develop algorithms to be executed in MapReduce involving numerical methods for analytics.

Suggested Evaluation Methods:
- Mini Project (Group) – Real time data collection, saving in NoSQL, implement analytical techniques using Map-Reduce Tasks and Result Projection.

TOTAL: 45 PERIODS
COURSE OUTCOMES:
On completion of the course, the student will be able to:
- Identify the real world business problems and model with analytical solutions.
- Solve analytical problems with relevant mathematics background knowledge.
- Convert any real world decision-making problem to hypothesis and apply suitable statistical testing.
- Write and demonstrate simple applications involving analytics using Hadoop and MapReduce.
- Use open source frameworks for modeling and storing data.
- Apply suitable visualization techniques using R for visualizing voluminous data.

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OE5092 INDUSTRIAL SAFETY L T P C 3 0 0 3

OBJECTIVES:
- Summarize basics of industrial safety
- Describe fundamentals of maintenance engineering
- Explain wear and corrosion
- Illustrate fault tracing
- Identify preventive and periodic maintenance

UNIT I INTRODUCTION
Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.
UNIT II  FUNDAMENTALS OF MAINTENANCE ENGINEERING  9
Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT III  WEAR AND CORROSION AND THEIR PREVENTION  9

UNIT IV  FAULT TRACING  9
Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment’s like, i. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT V  PERIODIC AND PREVENTIVE MAINTENANCE  9
Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: i. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

TOTAL: 45 PERIODS

COURSE OUTCOMES:
Students will be able to:
CO1: Ability to summarize basics of industrial safety
CO2: Ability to describe fundamentals of maintenance engineering
CO3: Ability to explain wear and corrosion
CO4: Ability to illustrate fault tracing
CO5: Ability to identify preventive and periodic maintenance

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REFERENCES:
OBJECTIVES:
- Solve linear programming problem and solve using graphical method.
- Solve LPP using simplex method
- Solve transportation, assignment problems
- Solve project management problems
- Solve scheduling problems

UNIT I LINEAR PROGRAMMING
Introduction to Operations Research – assumptions of linear programming problems - Formulations of linear programming problem – Graphical method

UNIT II ADVANCES IN LINEAR PROGRAMMING
Solutions to LPP using simplex algorithm- Revised simplex method - primal dual relationships – Dual simplex algorithm - Sensitivity analysis

UNIT III NETWORK ANALYSIS – I
Transportation problems -Northwest corner rule, least cost method, Voges’s approximation method - Assignment problem - Hungarian algorithm

UNIT IV NETWORK ANALYSIS – II
Shortest path problem: Dijkstra’s algorithms, Floyd’s algorithm, systematic method - CPM/PERT

UNIT V NETWORK ANALYSIS – III
Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models

TOTAL: 45 PERIODS

COURSE OUTCOMES:
Students will be able to:
CO1: To formulate linear programming problem and solve using graphical method.
CO2: To solve LPP using simplex method
CO3: To formulate and solve transportation, assignment problems
CO4: To solve project management problems
CO5: To solve scheduling problems

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REFERENCES:
OBJECTIVES:
- Summarize the costing concepts and their role in decision making
- Infer the project management concepts and their various aspects in selection
- Interpret costing concepts with project execution
- Develop knowledge of costing techniques in service sector and various budgetary control techniques
- Illustrate with quantitative techniques in cost management

UNIT I INTRODUCTION TO COSTING CONCEPTS 9
Objectives of a Costing System; Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost; Creation of a Database for operational control.

UNIT II INTRODUCTION TO PROJECT MANAGEMENT 9
Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities, Detailed Engineering activities, Pre project execution main clearances and documents, Project team: Role of each member, Importance Project site: Data required with significance, Project contracts.

UNIT III PROJECT EXECUTION AND COSTING CONCEPTS 9
Project execution Project cost control, Bar charts and Network diagram, Project commissioning: mechanical and process, Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis, Various decision-making problems, Pricing strategies: Pareto Analysis, Target costing, Life Cycle Costing.

UNIT IV COSTING OF SERVICE SECTOR AND BUDGETERY CONTROL 9
Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis, Budgetary Control: Flexible Budgets; Performance budgets; Zero-based budgets.

UNIT V QUANTITATIVE TECHNIQUES FOR COST MANAGEMENT 9
Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Learning Curve Theory.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
Students will be able to:
CO1 – Understand the costing concepts and their role in decision making
CO2–Understand the project management concepts and their various aspects in selection
CO3–Interpret costing concepts with project execution
CO4–Gain knowledge of costing techniques in service sector and various budgetary control techniques
CO5 - Become familiar with quantitative techniques in cost management
REFERENCES:
2. Charles T. Horngren and George Foster, Advanced Management Accounting, 1988

OE5095 COMPOSITE MATERIALS L T P C
3 0 0 3

OBJECTIVES:
- Summarize the characteristics of composite materials and effect of reinforcement in composite materials.
- Identify the various reinforcements used in composite materials.
- Compare the manufacturing process of metal matrix composites.
- Understand the manufacturing processes of polymer matrix composites.
- Analyze the strength of composite materials.

UNIT I INTRODUCTION
- Definition – Classification and characteristics of Composite materials - Advantages and application of composites - Functional requirements of reinforcement and matrix - Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT II REINFORCEMENTS
- Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers - Properties and applications of whiskers, particle reinforcements - Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures - Isostrain and Isostress conditions.

UNIT III MANUFACTURING OF METAL MATRIX COMPOSITES

UNIT IV MANUFACTURING OF POLYMER MATRIX COMPOSITES

UNIT V STRENGTH
- Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TOTAL: 45 PERIODS
COURSE OUTCOMES:
Students will be able to:
CO1 Know the characteristics of composite materials and effect of reinforcement in composite materials.
CO2 Know the various reinforcements used in composite materials.
CO3 Understand the manufacturing processes of metal matrix composites.
CO4 Understand the manufacturing processes of polymer matrix composites.
CO5 Analyze the strength of composite materials.

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OE5096 WASTE TO ENERGY L T P C
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OBJECTIVES:
• Interpret the various types of wastes from which energy can be generated
• Develop knowledge on biomass pyrolysis process and its applications
• Develop knowledge on various types of biomass gasifiers and their operations
• Invent knowledge on biomass combustors and its applications on generating energy
• Summarize the principles of bio-energy systems and their features

UNIT I INTRODUCTION TO EXTRACTION OF ENERGY FROM WASTE
Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT II BIOMASS PYROLYSIS
Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT III BIOMASS GASIFICATION
UNIT IV   BIOMASS COMBUSTION
Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT V   BIO ENERGY
Properties of biogas (Calorific value and composition), Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
Students will be able to:
CO1 Understand the various types of wastes from which energy can be generated
CO2 Gain knowledge on biomass pyrolysis process and its applications
CO3 Develop knowledge on various types of biomass gasifiers and their operations
CO4 Gain knowledge on biomass combustors and its applications on generating energy
CO5 Understand the principles of bio-energy systems and their features

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REFERENCES:

AUDIT COURSES (AC)

AX5091 ENGLISH FOR RESEARCH PAPER WRITING L T P C
2 0 0 0

OBJECTIVES
• Teach how to improve writing skills and level of readability
• Tell about what to write in each section
• Summarize the skills needed when writing a Title
• Infer the skills needed when writing the Conclusion
• Ensure the quality of paper at very first-time submission

UNIT I   INTRODUCTION TO RESEARCH PAPER WRITING
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness
UNIT II  PRESENTATION SKILLS  6

UNIT III  TITLE WRITING SKILLS  6
Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV  RESULT WRITING SKILLS  6
Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V  VERIFICATION SKILLS  6
Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first-time submission

TOTAL: 30 PERIODS

COURSE OUTCOMES
CO1 – Understand that how to improve your writing skills and level of readability
CO2 – Learn about what to write in each section
CO3 – Understand the skills needed when writing a Title
CO4 – Understand the skills needed when writing the Conclusion
CO5 – Ensure the good quality of paper at very first-time submission

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AX5092  DISASTER MANAGEMENT  L T P C  2 0 0 0

OBJECTIVES
- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT I  INTRODUCTION  6
Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.
UNIT II  REPERCUSSIONS OF DISASTERS AND HAZARDS

UNIT III  DISASTER PRONE AREAS IN INDIA
Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT IV  DISASTER PREPAREDNESS AND MANAGEMENT
Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V  RISK ASSESSMENT

TOTAL : 30 PERIODS

COURSE OUTCOMES
CO1: Ability to summarize basics of disaster
CO2: Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
CO3: Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
CO4: Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
CO5: Ability to develop the strengths and weaknesses of disaster management approaches

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OBJECTIVES
- Illustrate the basic sanskrit language.
- Recognize sanskrit, the scientific language in the world.
- Appraise learning of sanskrit to improve brain functioning.
- Relate sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power.
- Extract huge knowledge from ancient literature.

UNIT I  ALPHABETS  6
Alphabets in Sanskrit

UNIT II  TENSES AND SENTENCES  6
Past/Present/Future Tense - Simple Sentences

UNIT III  ORDER AND ROOTS  6
Order - Introduction of roots

UNIT IV  SANSKRIT LITERATURE  6
Technical information about Sanskrit Literature

UNIT V  TECHNICAL CONCEPTS OF ENGINEERING  6
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TOTAL: 30 PERIODS

COURSE OUTCOMES
- CO1 - Understanding basic Sanskrit language.
- CO2 - Write sentences.
- CO3 - Know the order and roots of Sanskrit.
- CO4 - Know about technical information about Sanskrit literature.
- CO5 - Understand the technical concepts of Engineering.

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REFERENCES
1. “Abhyaspustakam” – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. “Teach Yourself Sanskrit” Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
OBJECTIVES
Students will be able to
- Understand value of education and self-development
- Imbibe good values in students
- Let the should know about the importance of character

UNIT I

UNIT II

UNIT III

UNIT IV

TOTAL: 30 PERIODS

COURSE OUTCOMES
Students will be able to
- Knowledge of self-development.
- Learn the importance of Human values.
- Developing the overall personality.

SUGGESTED READING

AX5095 CONSTITUTION OF INDIA

OBJECTIVES
Students will be able to:
- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals’ constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.
UNIT I  HISTORY OF MAKING OF THE INDIAN CONSTITUTION:
History, Drafting Committee, (Composition & Working)

UNIT II  PHILOSOPHY OF THE INDIAN CONSTITUTION:
Preamble, Salient Features

UNIT III  CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES:
Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to
Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies,

UNIT IV  ORGANS OF GOVERNANCE:
Parliament, Composition, Qualifications and Disqualifications, Powers and Functions,
Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of
Judges, Qualifications, Powers and Functions.

UNIT V  LOCAL ADMINISTRATION:
District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and
role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI:
Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block
level: Organizational Hierarchy(Different departments), Village level: Role of Elected and
Appointed officials, Importance of grass root democracy.

UNIT VI  ELECTION COMMISSION:
Election Commission: Role and Functioning. Chief Election Commissioner and Election
Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS

COURSE OUTCOMES
Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the
  arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the
  conceptualization
- of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist
  Party(CSP) under the leadership of Jawaharlal Nehru and the eventual failure of the
  proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

SUGGESTED READING
1. The Constitution of India, 1950(Bare Act), Government Publication.

AX5096  PEDAGOGY STUDIES
L T P C  2 0 0 0

OBJECTIVES
Students will be able to:

- Review existing evidence on there view topic to inform programme design and policy
- Making under taken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.
UNIT I    INTRODUCTION AND METHODOLOGY:
Aims and rationale, Policy background, Conceptual framework and terminology - Theories of learning, Curriculum, Teacher education - Conceptual framework, Research questions - Overview of methodology and Searching.

UNIT II    THEMATIC OVERVIEW
Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries - Curriculum, Teacher education.

UNIT III    EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES
Methodology for the in depth stage: quality assessment of included studies - How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? - Theory of change - Strength and nature of the body of evidence for effective pedagogical practices - Pedagogic theory and pedagogical approaches - Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT IV    PROFESSIONAL DEVELOPMENT
Professional development: alignment with classroom practices and follow up support - Peer support - Support from the head teacher and the community - Curriculum and assessment - Barriers to learning: limited resources and large class sizes

UNIT V    RESEARCH GAPS AND FUTURE DIRECTIONS
Research design – Contexts – Pedagogy - Teacher education - Curriculum and assessment - Dissemination and research impact.

TOTAL: 30 PERIODS

COURSE OUTCOMES
Students will be able to understand:
- What pedagogical practices are being used by teachers informal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

SUGGESTED READING
AX5097 STRESS MANAGEMENT BY YOGA

OBJECTIVES
- To achieve overall health of body and mind
- To overcome stress

UNIT I
Definitions of Eight parts of yoga.(Ashtanga)

UNIT II
Yam and Niyam - Do’s and Don't’s in life - i) Ahinsa, satya, astheya, bramhacharya and aparigraha, ii) Ahinsa, satya, astheya, bramhacharya and aparigraha.

UNIT III
Asan and Pranayam - Various yog poses and their benefits for mind & body - Regularization of breathing techniques and its effects-Types of pranayam

TOTAL: 30 PERIODS

SUGGESTED READING
1. “Yogic Asanas for Group Tarining-Part-I”-Janardan Swami Yoga bhyasi Mandal, Nagpur
2. “Rajayoga or conquering the Internal Nature” by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

AX5098 PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

OBJECTIVES
- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

UNIT I
Neetisatakam-holistic development of personality - Verses- 19,20,21,22 (wisdom) - Verses-29,31,32 (pride & heroism) – Verses- 26,28,63,65 (virtue) - Verses- 52,53,59 (dont’s) - Verses-71,73,75,78 (do’s)

UNIT II
Approach to day to day work and duties - Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48 - Chapter 3-Verses 13, 21, 27, 35 Chapter 6-Verses 5,13,17,23, 35 - Chapter 18-Verses 45, 46, 48.

UNIT III
Statements of basic knowledge - Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 Chapter 12 -Verses 13, 14, 15, 16,17, 18 - Personality of role model - shrimad bhagwad geeta - Chapter2-Verses 17, Chapter 3-Verses 36,37,42 - Chapter 4-Verses 18, 38,39 Chapter18 – Verses 37,38,63

TOTAL: 30 PERIODS
COURSE OUTCOMES
Students will be able to
- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neet is hatakam will help in developing versatile personality of students.

SUGGESTED READING
1. Gopinath, Rashtriya Sanskrit Sansthanam P, Bhartrihari’s Three Satakam, Niti-sringar-vairagya, New Delhi, 2010