ANNA UNIVERSITY, CHENNAI
UNIVERSITY DEPARTMENTS
REGULATION – 2023
M.E APPLIED ELECTRONICS

VISION

To be recognized as a benchmark and trend setter in Electronics and Communication Engineering domain keeping in phase with rapidly changing technologies through effective partnership with reputed academic institutions, research organizations, industries and community.

MISSION

- Create highly motivated, technologically competent human resource by imparting high quality technical education through flexible student centric updated curricula suited to students with diverse backgrounds
- Adopt best teaching and learning practices and establish state-of-the-art facilities to provide quality academic ambience for innovativeness, research and developmental activities
- Enhance collaborative activities with academic institutions and industries for evolving indigenous technological solutions to meet societal needs and nurture leadership and entrepreneurship qualities with ethical means.
- Facilitate adequate exposure to the students, faculty and staff through training in the state-of-the-art technologies, efficient administration, global outreach and benchmarking against referential institutions
PROGRAMME EDUCATIONAL OBJECTIVES:

1. Graduates will expose technical problem solving skills with solid foundation in electronics, evolving advancements and remain committed for sustainable societal development.
2. Graduates will attain ability to excel in their future scope of career, research and role in engineering innovations by utilization of their electronics engineering foundation.
3. Graduates will develop skills for entrepreneurship, professional development and leadership in organizations by engaging in life-long learning process.

PROGRAM OUTCOMES:

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<th>PO#</th>
<th>Graduate Attribute</th>
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<tr>
<td>1.</td>
<td>Research aptitude</td>
<td>An ability to independently carry out research/investigation and development work to solve practical problems.</td>
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<td>2.</td>
<td>Technical documentation</td>
<td>An ability to write and present a substantial technical report/document.</td>
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<td>3.</td>
<td>Technical competence</td>
<td>Students should be able to demonstrate a degree of mastery over Applied Electronics.</td>
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<td>Engineering Design</td>
<td>An ability to apply various advanced tools and techniques of applied electronics to develop efficient hardware and software solutions.</td>
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<tr>
<td>5.</td>
<td>The engineer and society</td>
<td>Apply technical knowledge towards the development of socially relevant products.</td>
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MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMME OUTCOMES:

A broad relation between the programme objective and the outcomes is given in the following table:

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**TOTAL NO. OF CREDITS: 72**

## FOUNDATION COURSE (FC)

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## PROFESSIONAL CORE COURSES (PCC)

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## M.E APPLIED ELECTRONICS

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MA3152 ADVANCED APPLIED MATHEMATICS  L T P C
4 0 0 4

UNIT I  LINEAR ALGEBRA  12
Vector spaces – norms – Inner Products – Eigenvalues using QR transformations – QR factorization -
generalized eigenvectors – Canonical forms – singular value decomposition and applications - pseudo inverse – least square approximations --Toeplitz matrices and some applications.

UNIT II  ONE DIMENSIONAL RANDOM VARIABLES  12

UNIT III  RANDOM PROCESSES  12
Classification – Auto correlation - Cross correlation - Stationary random process – Markov process — Markov chain - Poisson process – Gaussian process.

UNIT IV  LINEAR PROGRAMMING  12
Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

UNIT V  FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS  12

TOTAL: 45+15=60 PERIODS

COURSE OUTCOMES:
At the end of the course, students will be able to
CO1 Apply the concepts of linear algebra to solve practical problems.
CO2 Use the ideas of probability and random variables in solving engineering problems.
CO3 Classify various random processes and solve problems involving stochastic processes.
CO4 Formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
CO5 Apply the Fourier transform methods of solving standard partial differential equations.

REFERENCES:
   Printice Hall of India, New Delhi, 2006.
   Boston, 2014.
RM3151 RESEARCH METHODOLOGY AND IPR

UNIT I RESEARCH PROBLEM FORMULATION
Objectives of research, types of research, research process, approaches to research; conducting literature review- information sources, information retrieval, tools for identifying literature, Indexing and abstracting services, Citation indexes, summarizing the review, critical review, identifying research gap, conceptualizing and hypothesizing the research gap

UNIT II RESEARCH DESIGN AND DATA COLLECTION
Statistical design of experiments- types and principles; data types & classification; data collection - methods and tools

UNIT III DATA ANALYSIS, INTERPRETATION AND REPORTING
Sampling, sampling error, measures of central tendency and variation; test of hypothesis-concepts; data presentation- types of tables and illustrations; guidelines for writing the abstract, introduction, methodology, results and discussion, conclusion sections of a manuscript; guidelines for writing thesis, research proposal; References – Styles and methods, Citation and listing system of documents; plagiarism, ethical considerations in research

UNIT IV INTELLECTUAL PROPERTY RIGHTS
Concept of IPR, types of IPR – Patent, Designs, Trademarks and Trade secrets, Geographical indications, Copy rights, applicability of these IPR; IPR & biodiversity; IPR development process, role of WIPO and WTO in IPR establishments, common rules of IPR practices, types and features of IPR agreement, functions of UNESCO in IPR maintenance.

UNIT V PATENTS
Patents – objectives and benefits of patent, concept, features of patent, inventive steps, specifications, types of patent application; patenting process - patent filling, examination of patent, grant of patent, revocation; equitable assignments; Licenses, licensing of patents; patent agents, registration of patent agents.

TOTAL: 45 PERIODS

COURSE OUTCOMES
Upon completion of the course, the student can
CO1: Describe different types of research; identify, review and define the research problem
CO2: Select suitable design of experiments; describe types of data and the tools for collection of data
CO3: Explain the process of data analysis; interpret and present the result in suitable form
CO4: Explain about Intellectual property rights, types and procedures
CO5: Execute patent filing and licensing
REFERENCES:
2. Soumitro Banerjee, “Research methodology for natural sciences”, IISc Press, Kolkata, 2022,

AP3101 EMBEDDED SYSTEM DESIGN L T P C
3 0 4 5

UNIT I EMBEDDED COMPUTING PLATFORM – HARDWARE ASPECT 9

UNIT II EMBEDDED COMPUTING PLATFORM – SOFTWARE ASPECT 9

UNIT III DISTRIBUTED EMBEDDED COMPUTING PLATFORM 9
Multiprocessors- CPUs and Accelerators – Performance Analysis- Distributed Embedded Architecture – Networks for Embedded Systems: - I²C Bus, CAN Bus, SHARC Link Port-Ethernet, Myrinet – Network based design – Internet enabled systems-Network based system performance Analysis

UNIT IV ARM PROCESSOR 9

UNIT V SYSTEM DESIGN – APPLICATION CASE STUDY 9

THEORY: 45 PERIODS

PRACTICAL EXERCISES: 1. Push button, LED, LCD display and RTC interfacing with AVR RISC based microcontroller.

LAB: 60 PERIODS
2. AVR RISC based Microcontroller system design with Touch screen interfacing.
4. Interfacing sensors and RFID with AVR RISC based Microcontroller.
5. Design of RC5 remote control decoder with AVR RISC based Microcontroller.
6. Implementing I2C, SPI, CAN and UART protocols with ARM 7 processor.
7. Design and implementation of path tracking and obstacle avoidance Robot.
9. Design and implementation of Robotic Arm manipulation with 6 DOF.
10. Design and implementation of Pick and Place robot.
11. Design and implementation of color and pattern guided material handling robot.
12. Design and implementation of human detection robot using PIR sensor.

COURSE OUTCOMES:

CO1: Ability to apply the hardware design concepts in developing an embedded system.
CO2: Ability to apply the software aspects embedded system design
CO3: Ability to apply networking principles in embedded devices using EDA tools, sensor, high power devices and motors effectively.
CO4: Ability to understand and use ARM processors in implementing embedded devices.
CO5: Ability to design suitable embedded systems for real world applications and demonstrate competence in working with different Robot Operating Systems(ROS).

REFERENCES:


TOTAL: 105 PERIODS

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UNIT I  INTRODUCTION TO RANDOM SIGNAL PROCESSING  9
Discrete Random Processes- Ensemble Averages, Stationary processes, Bias and Estimation, 
Autocovariance, Autocorrelation, Parseval's theorem, Wiener-Khintchine relation, White noise, 

UNIT II  SIGNAL MODELING  9
ARMA (p,q), AR (p), MA (q) models, Forward Linear Prediction, Backward Linear Prediction: 
– Yule-Walker Method, Solution to Prony’s normal equation, Levinson Durbin Algorithm.

UNIT III  SPECTRAL ESTIMATION  9
Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified 
periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric method, AR 
(p) spectral estimation and detection of Harmonic signals.

UNIT IV  LINEAR ESTIMATION  9
Linear Minimum Mean-Square Error (LMMSE) Filtering: Wiener Hopf Equation, FIR Wiener filter, 
Noise Cancellation, Causal IIR Wiener filter, Non-causal IIR Wiener filter.

UNIT V  ADAPTIVE FILTERS  9
FIR adaptive filters — adaptive filter based on steepest descent method- Widrow-Hopf LMS 
algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo 
cancellation, Adaptive noise cancellation, RLS adaptive algorithm.

TOTAL: 45 PERIODS

PRACTICAL EXERCISES:  LAB: 60 PERIODS
Tools: any tool, MATLAB, SIMULINK, LABVIEW, any processor.

(Use only filtering and adaptive filtering, statistical analysis, feature extraction etc. Don’t use 
machine learning, deep learning, AI, NN, CNN)

1. Simulate sum of three sinusoidal signals. Add white noise with various noise density and try to 
remove noise using appropriate filter. Try to find various statistical features and compare. Plot 
(i) I/P and O/P signal without noise in time domain and frequency domain (ii) I/P and O/P signal 
with noise in time domain and frequency domain

2. Try to record your voice in an ideal condition. Add noise with various noise density. Recover 
your signal using noise removal algorithm, i.e., using various filter. Try to find various statistical 
features and compare. Plot (i) I/P and O/P signal without noise in time domain and frequency 
domain (ii) I/P and O/P signal with noise in time domain and frequency domain

3. Try to record all your (Classmates) voices. Try to separate each of the voice from mixed of all 
voices. Assumptions you can made

4. Try to say or sing the same line, Pick the signal(s) in the ideal environment, Pick the signal(s) in 
the noisy environment (known noise or unknown noise(noise can be added by picking the signal 
when all the fans in the room are running))
5. Take any song of your choice. Try to separate each of the component in that song. (Music instruments, voice, etc). If possible add noise and try to recover the original song.

6. Pick different bird sounds (separately and mixed together) (with and without noise) (if possible in our campus). Try to label it.

7. Do the same as in question 4 for different animals.

8. Try to do the same in question 2, for different age groups (ex: age 4 to age 80).

**COURSE OUTCOMES:**

**CO1:** Ability to analyze discrete time random processes.

**CO2:** Ability to obtain models for prediction and Estimation.

**CO3:** Ability to analyze non-parametric methods and parametric methods for spectral estimation.

**CO4:** Ability to design different MMSE filters and adaptive filters for different applications.

**CO5:** Ability to develop a system for real time applications using any tool.

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**AP3151 ANALOG INTEGRATED CIRCUIT DESIGN**

**UNIT I SINGLE STAGE AMPLIFIERS**

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower differential with active load, Cascode and folded Cascode configurations with active load, Design of differential and Cascode amplifiers – to meet specified SR, gain, BW, ICMR and power dissipation, voltage swing, High gain amplifier, structures.
UNIT II HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS
Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, Cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III NEGATIVE FEEDBACK AMPLIFIERS AND OPERATIONAL AMPLIFIERS
Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage OpAmps, Two-stage OpAmps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in OpAmps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE OPERATIONAL AMPLIFIER
Analysis of two stage OpAmp – two stage OpAmp single stage CMOS CS as second stage and using Cascode second stage, multiple systems, Phase Margin, Frequency Compensation, and Compensation of two stage OpAmps, Slew in two stage OpAmps, Other compensation techniques.

UNIT V VOLTAGE AND CURRENT REFERENCES
Current sinks and sources, Current mirrors, Wilson current source, Widlar current source, Cascode current source, Design of high swing Cascode sink, Current amplifiers, Supply independent biasing, temperature independent references, PTAT and CTAT current generation, Constant-Gm Biasing.

TOTAL: 45 PERIODS

PRACTICAL Exercises:
1. Extraction of process parameters of CMOS process Transistors
   a. Plot ID vs. VGS at different drain voltages for nMOS, PMOS.
   b. Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
   c. Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
   d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
2. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
   a. Calculate input bias voltage for a given bias current.
   b. Use spice and obtain the bias current. Compare with the theoretical value
   c. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in spice, considering load capacitance.
   d. Plot step response of the amplifier with a specific input pulse amplitude. Derive time constant of the output and compare it with the time constant resulted from -3dB BW.
   e. Use spice to determine input voltage range of the amplifier.
3. Realize layout and perform post layout simulation of the CS amplifier realized in Ex.No.2
4. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter
   a. Perform DC analysis and determine input common mode range and compare with the theoretical values.
   b. Perform time domain simulation and verify low frequency gain.
   c. Perform AC analysis and verify low-frequency voltage gain and unity gain BW (fu)
5. Stability Analysis of Two stage OpAmp
   a. Perform DC analysis and determine input common mode range and compare with the theoretical values.
   b. Perform time domain simulation and verify low frequency gain.
   c. Perform AC analysis and verify low-frequency voltage gain and unity gain BW (fu)

COURSE OUTCOMES:
CO1: Ability to design amplifiers to meet user specifications
CO2: Ability to analyse the frequency and noise performance of amplifiers
CO3: Ability to design and analyse negative feedback amplifiers and opAmps
CO4: Ability to analyse stability aspects of two stage opAmps
CO5: Ability to design and use current mirrors, current sources using MOS devices

REFERENCES:
UNIT III  FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS  

UNIT IV  SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES  

UNIT V  SYSTEM DESIGN USING VERILOG  

TOTAL: 45 PERIODS

COURSE OUTCOMES:  
CO1: Ability to analyse and design synchronous sequential circuits.  
CO2: Ability to analyse hazards and design asynchronous sequential circuits.  
CO3: Ability to apply the testing procedure for combinational circuit and PLA.  
CO4: Able to design PLD and ROM.  
CO5: Ability to design and use programming tools for implementing digital circuits.

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UNIT I  BASICIS OF PCB DESIGN, TOOLS & INDUSTRY STANDARDS
Printed Circuit Board Fabrication - PCB cores and layer stack-up. PCB fabrication process - Photolithography and chemical etching, Mechanical milling and Layer registration. Function of the Layout in the PCB Design Process. Design Files Created by Layout - Layout format files, Postprocess (Gerber) files, PCB assembly layers and files. Introduction to the Standards Organizations, Classes and Types of PCBs, Introduction to Standard Fabrication Allowances, PCB Dimensions and Tolerances, Copper Trace and Etching Tolerances, Standard Hole Dimensions, Soldermask Tolerance.

UNIT II  PCB DESIGN FLOW USING CAD TOOL
Overview of Computer-Aided Design. Setting up the user account, Starting a new project, Schematic Entry, Placing and wiring (connecting) the parts, Converting Schematic to Layout, Layout Environment and Tool Set, Designing the PCB with Layout – Setting constraints, Placing the parts, Auto routing and the Manual routing, Performing a design rule check, Making a board outline, Post processing the board design for manufacturing, Submitting Gerber files and requesting a quote, Annotating the layer types and stack-up, Receipt inspection and testing, Nonstandard Gerber files.

UNIT III  DESIGN CONSTRAINTS FOR MANUFACTURING
PCB Assembly and Soldering Processes - Component Placement and Orientation Guide, Component Spacing for Through-hole Devices (THDs). Component Spacing for Surface Mounted Devices (SMDs), Mixed THD and SMD Spacing Requirements. Footprint and Pad stack Design for PCB Manufacturability- Land Patterns for SMDs- Land Patterns for THDs, Pad stack design, Hole-to-lead ratio, PTH land dimension (annular ring width), Clearance between plane layers and PTHs Solder mask and solder paste dimensions.

UNIT IV  PCB DESIGN FOR SIGNAL INTEGRITY

UNIT V  EMERGING PCB FABRICATION PROCESSES

PRACTICAL EXERCISES:
1. Schematic capture using EDA tool.
2. Prepare PCB design layout and generate Gerber files and other files formats.
3. Design and fabrication of single layer PCB using traditional method.
4. PTH and via drilling in PCB by manual and automated (Bantam tools) methods.
5. Mechanical registration and riveting of PTH and via.
6. Design and fabrication of double layer PCB using laser technology.
7. Design and fabrication of PCB using Bantam tools (milling process).

TOTAL: 45 PERIODS
LAB: 60 PERIODS
8. Design and fabrication of PCB using Voltera V-one machine.
10. SMD placing on PCB using pick and place machine.
11. PCB assembly of SMD using reflow soldering with temperature profiling of reflow oven.
12. PCB assembly of THD using manual and robotic soldering.
13. PCB assembly of THD using Wave soldering and its temperature profiling.
14. Design and fabricate PCB for AVR RISC based microcontroller development board.
15. Perform PCB assembly in the microcontroller development board.
16. Optical inspection and Verification of the microcontroller development board.
17. Conductive emission and Radiative emission test for PCB.

TOTAL: 105 PERIODS

COURSE OUTCOMES
At the end of the course students will be able to:

CO1: To understand the basics, industry standards organizations related to the design and fabrication of PCBs by using EDA tools.

CO2: Leads new users of the software through a very simple design.

CO3: To know and guide in designing plated through-holes, surface-mount lands, and Layout footprints in general while designing a schematic diagram.

CO4: To know to construct Capture parts using the Capture Library Manager and Part Editor and the PSpice Model Editor.

CO5: To understand and to fabricate PCBs by different fabrication methods.

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UNIT I  MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER  12
MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter-Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, Stick diagram and Layout diagrams.

UNIT II  COMBINATIONAL LOGIC CIRCUITS  9
Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Interconnect Delay, Dynamic Logic Gates.

UNIT III  SEQUENTIAL LOGIC CIRCUITS  9
Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Nonbistable Sequential Circuits.

UNIT IV  ARITHMETIC BUILDING BLOCKS  9
Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs

UNIT V  MEMORY ARCHITECTURES  6
Memory Architectures and Memory control circuits: Read-Only Memories, ROM cells, Read- write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: To be able to use mathematical methods and circuit analysis models in analysis of CMOS digital circuits.
CO2: To be able to create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort.
CO3: To be able to design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches.
CO4: To be able to learn design methodology of arithmetic building blocks.
CO5: To be able to design functional units including ROM and SRAM.

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AP3211 SIGNAL PROCESSING SYSTEM DESIGN LABORATORY  L T P C
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LIST OF EXPERIMENTS:
1) HDL realization and timing analysis of
   i. Combinational circuits namely 8:1 Mux/Demux, Full Adder, 8-bit Magnitude
comparator, Encoder/decoder, Priority encoder.
   ii. Sequential circuits namely D-FF, 4-bit Shift registers (SISO, SIPO, PISO,
bidirectional), 3-bit Synchronous Counters.
2) FPGA implementation of PCI Bus & arbiter.
3) Realization of UART/ USART implementation in HDL and design validation using test vector
generation.
4) FPGA realization of single port SRAM and capturing the signal in DSO.
5) Back annotation and timing analysis of Arithmetic circuits like serial adder/subtractor,
parallel adder/subtractor, serial/parallel multiplier.
6) Realization of Discrete Fourier transform/Fast Fourier Transform algorithm in HDL and
observing the spectrum in simulation.
7) Design and implement FIR and IIR filters.
8) Design and implement adaptive filters.

COURSE OUTCOMES:
At the end of the course students will be able to:
CO1: Ability to identify, formulate, solve and implement problems in signal processing,
communication systems etc using RTL design tools.
CO2: Ability to validate the design in FPGA starting from design entry to back annotation.
CO3: Ability to use EDA tools like Cadence/Mentor Graphics/ Xilinx/Altera Quartus.
CO4: Ability to develop Fourier Transform algorithm in HDL.
CO5: Ability to implement filters using HDL.

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UNIT I  DIGITAL IMAGE FUNDAMENTALS  12
Image Acquisition, Elements of visual perception, Image sampling, Quantization, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform, Simulation of basic image processing operations using mathematical tools and image transforms.

UNIT II  IMAGE ENHANCEMENT AND RESTORATION  12

UNIT III  IMAGE SEGMENTATION AND MORPHOLOGY  12
Image segmentation - Edge detection, Edge linking, Thresholding, Region growing, Region splitting and Merging, Morphological Image Processing - Basics, SE, Erosion, Dilation, Opening, Closing, Hit-or-Miss Transform, Boundary Detection, Hole filling, Connected components, convex hull, thinning, thickening, skeletons, pruning, Geodesic Dilation, Erosion, Reconstruction by dilation and erosion. Simulation of Canny edge detection, Otsu Thresholding and Morphological operations.

UNIT IV  IMAGE COMPRESSION  12
Lossless and Lossy compression: Variable length coding, LZW, transform coding, JPEG and MPEG compression standards. Simulation of coding techniques.

UNIT V  FEATURE EXTRACTION AND PATTERN CLASSIFICATION  12
Boundary Representation - Chain codes, Boundary Descriptors, Region Descriptors, Scale-invariant Feature Transform Features, Speed-up Robust Features, Principal Components.Object Recognition - Patterns and pattern classes, Prototype Matching by minimum distance classifier, Matching by correlation, Optimum Bayes Statistical Classifiers. Case study on image segmentation and classification for real-world applications.

TOTAL: 60 PERIODS

COURSE OUTCOMES:
CO1: Ability to analyze image acquisition and apply transforms specific to applications.
CO2: Ability to apply enhancement in both spatial and frequency domain and implement algorithms to restore degraded images.
CO3: Ability to develop and apply algorithms to extract objects of interest in images
CO4: Ability to apply image compression algorithms
CO5: Ability to interpret extracted object and its use in recognition.

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AP3002 DSP INTEGRATED CIRCUITS L T P C 3 0 0 3

UNIT I INTRODUCTION TO DSP INTEGRATED CIRCUITS 9
Sampling of analog signals, Selection of sample frequency, Signal processing systems,
Frequency response, Transfer functions, FFT-The Fast Fourier Transform Algorithm, Discrete
cosine transforms. Image coding, Adaptive DSP algorithms, Standard digital signal processors,
Application specific IC’s for DSP, DSP system design, Integrated circuit design.

UNIT II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 12
FIR filters, FIR filter structures, IIR filters, Specifications of IIR filters, Mapping of analog transfer
functions, Signal flow graphs, Filter structures, Mapping of analog filter structures, Finite word
length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off
noise, Coefficient sensitivity, Sensitivity and noise. Multirate systems, Interpolation with an integer
factor L, Sampling rate change with a ratio L/M, Multirate filters.

UNIT III DSP ARCHITECTURES 9
DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture.
TMS320C54x and TMS320C6x architecture, Multiprocessors and multicomputers, Systolic and
Wave front arrays, Shared memory architectures.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES & ARITHMETIC UNIT 9
Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs,
Shared memory architecture with Bit — serial PEs.
Arithmetic Unit : Conventional number system, Redundant Number system, Residue Number
System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift
accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator.

UNIT V CASE STUDY-INTEGRATED CIRCUIT DESIGN 6
Layout of VLSI circuits, Layout Styles, Case Study: FFT processor, DCT processor and
Interpolator.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to analyze and design fundamental signal processing algorithms and systems.
CO2: Adequacy to design and analyze digital filter concepts and structures.
CO3: Equipped to design general purpose digital signal processors.
CO4: Ability to use various implementation strategies for signal processing algorithms.
CO5: Equipped to design signal processing VLSI systems.

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AP3054 NONLINEAR SIGNAL PROCESSING L T P C 3 0 0 3
UNIT I INTRODUCTION TO NONLINEAR FILTERS AND STATISTICAL PRELIMINARIES 9

UNIT II NON LINEAR DIGITAL SIGNAL PROCESSING BASED ON ORDER STATISTICS 9

UNIT III ADAPTIVE NONLINEAR AND POLYNOMIAL FILTERS 9

Attested
DIRECTOR
Centre for Academic Courses
Anna University, Chennai-600 025
UNIT IV ALGORITHMS AND ARCHITECTURES

UNIT V APPLICATIONS OF NONLINEAR FILTERS
Power spectrum analysis – Morphological image processing – nonlinear edge detection impulse noise rejection in image and bio signals – two component image filtering – speech processing

TOTAL: 45 PERIODS

COURSE OUTCOMES
CO1: Ability to evaluate the characteristics of nonlinear filters
CO2: Ability to design and implement rank order filters.
CO3: Ability to develop polynomial filters.
CO4: Ability to design architectures for nonlinear filters.
CO5: Ability to implement nonlinear filters for different types of signals.

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AP3003 ADVANCED DIGITAL CONTROL ENGINEERING

UNIT I PRINCIPLES OF CONTROLLERS
Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL
Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.
UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM 9
Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9
Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9
Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to understand the concepts of discrete system science related mathematics and principles of controllers.
CO2: Ability to explain the discrete system, component or process to meet desired needs for signal processing in digital control systems.
CO3: Ability to understand the Z-transform to process time sequences and solve difference equations to characterize the stability, frequency response, transient time response and steady-state error of a digital control system.
CO4: Ability to design digital controllers in the z-domain and by approximation of S-domain design to solve discrete control engineering problems.
CO5: Ability to understand the techniques, tools and skills related to discrete signals, computer science and modern discrete control engineering in modern engineering practice.

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UNIT I  EMBEDDED ‘C’  

UNIT II  OBJECT ORIENTED PROGRAMMING  
Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

UNIT III  CPP PROGRAMMING  
‘cin’, ‘cout’, formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, ‘this’ pointer, constructors, destructors, friend function, dynamic memory allocation

UNIT IV  OVERLOADING AND INHERITANCE  
Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions

UNIT V  TEMPLATES  
Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions. Scripting Languages: Overview of Scripting Languages — PERL, CGI, VB Script, Java Script. PERL

COURSE OUTCOMES:
CO1: Ability to write an embedded C application of moderate complexity.
CO2: Ability to develop and analyze algorithms in C++.
CO3: Ability to differentiate interpreted languages from compiled languages.
CO4: Ability to differentiate the concepts of overloading and inheritance.
CO5: Ability to develop templates for different scripting languages.

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UNIT I THEORY OF PARALLELIS 9
Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.

UNIT II PARTITIONING AND SCHEDULING 9
Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

UNIT III HARDWARE TECHNOLOGIES 9
Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory — Bus Arbitration, cache memory organisations, shared memory organisations, sequential and weak consistency models.

UNIT IV PIPELINING, SUPERSCALAR, PARALLEL AND SCALABLE ARCHITECTURE 9

UNIT V MULTIVECTOR AND SIMD COMPUTERS 9

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Able to build up on advanced concepts of parallel architecture.
CO2: Able to design parallel architectures for improved performance
CO3: Ability to apply memory hierarchy for multiprocessor system.
CO4: Able to analyze the design structures of pipelined systems.
CO5: Able to analyze and design multiprocessor systems.

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AP3006 DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS

UNIT I INTRODUCTION

UNIT II DATA STRUCTURES
Introduction to Data Structures — Linear and Non-linear Data Structures — Lists — Stack — Queue — Graph — Tree — Data Structure Operations - Shortest Path Algorithms — MinimalSpanning Tree Construction.

UNIT III ALGORITHMS ANALYSIS AND DESIGN TECHNIQUES

UNIT IV SEARCHING AND SORTING

UNIT V NP-COMPLETE PROBLEMS

TOTAL: 45 PERIODS

COURSE OUTCOMES:
At the end of the course students will be able to:
CO1: Understand the Principles of Algorithms and Models of Computation.
CO2: Understand the Principles of Data Structures and its Applications.
CO3: Analyze and Design of Various Algorithms.
CO4: Create and Analyze Various Searching and Sorting Algorithms.
CO5: Understand the Principles of NP-Complete Problems.

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AP3058 WIRELESS SENSOR NETWORKS L T P C 3 0 0 3

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9

UNIT II ARCHITECTURES 9

UNIT III MAC AND ROUTING 9

UNIT IV INFRASTRUCTURE ESTABLISHMENT 9
Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT V DATA MANAGEMENT AND SECURITY 9
Data management in WSN, Storage and indexing in sensor networks, Query processing in sensor,
Data aggregation, Directed diffusion, Tiny aggregation, greedy aggregation, security in WSN, Case studies using simulation tools.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to design implement simple wireless network concepts.
CO2: Ability to design, analyze implement different network architectures
CO3: Ability to implement MAC layer and routing protocols.
CO4: Ability to deal with timing and control issues in wireless sensor networks
CO5: Ability to analyze and design secured wireless sensor networks.

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AP3007 IOT SYSTEM DESIGN AND SECURITY L T P C
3 0 0 3

UNIT I INTRODUCTION TO INTERNET OF THINGS 9
Rise of the machines – Evolution of IoT – Web 3.0 view of IoT – Definition and characteristics of IoT – Physical design of IoT – Logical design of IoT – IoT enabling technologies – IoT levels and deployment templates – A panoramic view of IoT applications.

UNIT II ARCHITECTURE OF IoT 9
Identification and Access to objects and services in the IoT environment( Current technologies for
IoT naming-Solutions proposed by research projects-Research and Future development trends and forecast) – Middleware technologies for IoT system (IoT Ecosystem Overview – Horizontal Architecture Approach for IoT Systems-SOA-based IoT Middleware)Middleware architecture of RFID, WSN, SCADA, M2M– Challenges Introduced by 5G in IoT Middleware (Technological Requirements of 5G Systems-5G-based IoT Services and Applications Requirements-5G-based Challenges for IoT Middleware) - Perspectives and a Middleware Approach Toward 5G (COMPaaS Middleware) – Resource management in IoT.

UNIT III SECURITY CONSIDERATIONS IN IOT SMART AMBIENT SYSTEMS

UNIT IV IOT ENABLERS AND THEIR SECURITY AND PRIVACY ISSUES
Internet of Things layer wise Protocols and Standards- EPC global (architecture, specifications, industry adaptation, security and vulnerabilities, advantages and disadvantages)- Wireless HART-ZigBee-Near Field Communication-6LoWPAN-Dash7-Comparative Analysis.

UNIT V APPLICATIONS AND CASE STUDIES

TOTAL: 45 PERIODS

COURSE OUTCOMES:
At the end of the course students will be able to:
CO1: Articulate the main concepts, key technologies, strength and limitations of IoT
CO2: Identify the architecture, infrastructure models of IoT.
CO3: Analyze the core issues of IoT such as security, privacy and interoperability.
CO4: Analyze and design different models for network dynamics.
CO5: Identify and design the new models for market strategic interaction.

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AP3051  ADVANCED MICROPROCESSORS AND MICROCONTROLLERS  L  T  P  C
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UNIT I  MICROPROCESSOR ARCHITECTURE  9

UNIT II  HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM  9

UNIT III  HIGH PERFORMANCE RISC ARCHITECTURE – ARM  9
Organization of CPU — Bus architecture – Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV  MSP430 16 - BIT MICROCONTROLLER  9

UNIT V  PIC MICROCONTROLLER  9

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to learn the fundamentals of microprocessor architecture.
CO2: Ability to know and appreciate the high performance features in CISC architecture.
CO3: Ability to know and appreciate the high performance features in RISC architecture.
CO4: Ability to perceive the basic features in Motorola microcontrollers.
CO5: Ability to interpret and understand PIC Microcontroller.

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AP3052  
ELECTRONICS FOR SOLAR POWER  
L T P C  
3 0 0 3

UNIT I  
INTRODUCTION TO SOLAR POWER  
9
Semiconductor – properties - energy levels - basic equations of semiconductor devices physics - Basic characteristics of sunlight - Solar angles - day length - angle of incidence on tilted surface — Sun path diagrams — Equivalent circuit of PV cell, PV cell characteristics (VI curve, PV curve) - Maximum power point, $V_{mp}, I_{MP}, V_{oc}, I_{sc}$ – types of PV cell - Block diagram of solar photo voltaic system, PV array sizing.

UNIT II  
DC-DC CONVERTER  
9
Principles of step-down and step-up converters – Analysis and design issues of buck, boost, buck-boost and Cuk converters – time ratio and current limit control – Case Study: Solar power based power system design with converters.

UNIT III  
MAXIMUM POWER POINT TRACKING  
9

UNIT IV  
BATTERY  
9
Types of Battery, Battery Capacity — Units of Battery Capacity-impact of charging and discharging rate on battery capacity-Columbic efficiency-Voltage Efficiency, Charging – Charge Efficiency, Charging methods, State of Charge, Charging Rates, Discharging - Depth of discharge-Discharge Methods, selection of Battery and sizing, Case study: Electric vehicle Battery Management System (EV-BMS).

UNIT V  
SIMULATION OF PV MODULE & CONVERTERS  
9
Matalb Simulation of PV module - VI Plot, PV Plot, finding $V_{mp}, I_{MP}, V_{oc}, I_{sc}$ of PV module, Simulation of DC to DC converter -buck, boost, buck-boost and Cuk converters, standalone and grid tied photo voltaic system. FPGA based design and simulation of MPPT controllers.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to collect solar power characteristics at a given location.
CO2: Ability to design and realize dc-dc converters for solar power utilization
CO3: Ability to design algorithms for improving solar power utilization.
CO4: Ability to deal with battery issues and selection.
CO5: Ability to design and simulate PV systems to validate its performance.

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AP3056  ROBOTICS AND INTELLIGENT SYSTEMS  L T P C  3 0 0 3

UNIT I  INTRODUCTION
Basic Concepts such as Definition, three laws, DOF, Misunderstood devices etc., Elements of Robotic Systems i.e. Robot anatomy, Classification, Associated parameters i.e. resolution, accuracy, repeatability, dexterity, compliance, RCC device, etc. Automation-Concept, Need, Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations, introduction to automation productivity.

UNIT II  ROBOT GRIPPERS
Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system. Sensors for Robots:- Characteristics of sensing devices, Selections of sensors, Classification and applications of sensors. Types of Sensors, Need for sensors and vision system in the working and control of a robot.

UNIT III  DRIVES AND CONTROL SYSTEMS

UNIT IV  MACHINE VISION SYSTEM
Vision System Devices, Robot Programming:- Methods of robot programming, lead through programming, motion interpolation, branching capabilities, WAIT, SIGNAL and DELAY commands,
subroutines. Programming Languages: Introduction to various types such as RAIL and VAL II etc, Features of type and development of languages for recent robot systems.

UNIT V MODELING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION 9

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to implement simple concepts associated with Robotics and Automation.
CO2: Ability to use various Robotic sub-systems.
CO3: Ability to use kinematics and dynamics to design exact working pattern of robots.
CO4: Ability to implement computer vision algorithms for robots.
CO5: Be aware of the associated recent updates in Robotics.

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AP3055 RF INTEGRATED CIRCUIT DESIGN L T P C 3 0 0 3

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES
Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up conversion Transmitter, Two step up conversion Transmitter.
UNIT II  IMPEDANCE MATCHING AND AMPLIFIERS  9
S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III  FEEDBACK SYSTEMS AND POWER AMPLIFIERS  9
Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model — Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT IV  MIXERS AND OSCILLATORS  9
Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V  PLL AND FREQUENCY SYNTHESIZERS  9
Linearized Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to explore user specifications for RF systems
CO2: Ability to analyze and design RF low noise amplifiers.
CO3: Ability to analyze and design RF power amplifiers.
CO4: Ability to analyze and design RF mixers and oscillators
CO5: Ability to design PLL for RF applications.

REFERENCE BOOKS:
5. Recorded lectures and notes available at http://www.ee.iitm.ac.in/~ani/ee6240/

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UNIT I  SIGNAL PROPAGATION ON TRANSMISSION LINES  9
Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations — L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline. Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin- effect, dispersion.

UNIT II  MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK  9
Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far- end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

UNIT III  NON-IDEAL EFFECTS  9
Non-ideal signal return paths — gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses — Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

UNIT IV  POWER CONSIDERATIONS AND SYSTEM DESIGN  9
SSN/SSO , DC power bus design , layer stack up, SMT decoupling , Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V  CLOCK DISTRIBUTION AND CLOCK OSCILLATORS  9
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to identify sources affecting the speed of digital circuits.
CO2: Ability to identify methods to improve the signal transmission characteristics
CO3: Ability to analyze non-ideal effects
CO4: Ability to analyze system power dissipation
CO5: Ability to analyze clocking strategies.

REFERENCES

TOOLS REQUIRED
1.  SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html

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AP3053  EMI AND EMC IN SYSTEM DESIGN  L T P C  3 0 0 3

UNIT I EMI/EMC CONCEPTS  9
EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES  9
Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling, cross talk; Field to cable coupling; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES  9
Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBs  9
Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations

UNIT V EMI MEASUREMENTS AND STANDARDS  9
Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx/Rx Antennas, Sensors, Injectors/ Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to gain knowledge to understand the concept of EMI / EMC related to product design & development.
CO2: Ability to analyze the different EM coupling principles and its impact on performance of electronic system.
CO3: Ability to analyze electromagnetic interference, highlighting the concepts of both susceptibility and immunity
CO4: Ability to interpret various EM compatibility issues with regard to the design of PCBs and ways to improve the overall system performance
CO5: Ability to obtain broad knowledge of various EM radiation measurement techniques and the present leading edge industry standards in different countries
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AP3008 ARTIFICIAL INTELLIGENCE AND OPTIMIZATION TECHNIQUES  L T P C 3 0 0 3

UNIT I  NEURAL NETWORKS 9

UNIT II  FUZZY LOGIC SYSTEMS 9

UNIT III  EVOLUTIONARY COMPUTATION & GENETIC ALGORITHMS 9

UNIT IV  ANT COLONY OPTIMIZATION 9
Ant Colony Optimization: Introduction — From real to artificial ants- Theoretical considerations — Convergence proofs — ACO Algorithm — ACO and model based search — Application principles of ACO.

UNIT V  PARTICLE SWARM OPTIMIZATION 9
Particle Swarm Optimization: Introduction — Principles of bird flocking and fish schooling — Evolution of PSO — Operating principles — PSO Algorithm — Neighborhood Topologies —
Convergence criteria – Applications of PSO, Honey Bee Social Foraging Algorithms, Bacterial Foraging Optimization Algorithm.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to design and train neural networks with different rules.
CO2: Ability to devise fuzzy logic rules.
CO3: Ability to implement genetic algorithms.
CO4: Ability to implement ANT colony optimization technique for various problems.
CO5: Ability to use PSO technique.

REFERENCES:
3. Christopher M. Bishop, “Neural Networks for Pattern Recognition”, Oxford University Press, 1995

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AP3009 NANOELECTRONICS L T P C 3 0 0 3

UNIT I INTRODUCTION TO NANO ELECTRONICS 9
Scaling to nano-Light as a wave and particle- Electrons as waves and particles- origin of quantum mechanics-General postulates of quantum mechanics-Spin and angular momentum-Wave packets and uncertainty.

UNIT II ELECTRONS CONFINEMENT IN LOW DIMENSIONAL STRUCTURES 9
Statistics of the electrons in solids and nanostructures, Density of states in nanostructures, Time independent Schrodinger wave equation- Electron confinement-Quantum dots, electron
UNIT III GROWTH, FABRICATION AND MEASUREMENT TECHNIQUES FOR NANOSTRUCTURES
Bulk crystal and heterostructure growth, Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices, Techniques for characterization of nanostructures (SEM, AFM, TEM), Spontaneous formation and ordering of nanostructures, Clusters and nanocrystals.
Methods of nanotube growth, Chemical and biological methods for nanoscale fabrication, Fabrication of nano electron mechanical systems.

UNIT IV NANOELECTRONICS DEVICES
Coulomb blockade- Single electron transistors, Semiconductor nanowire SETs, Field-effect transistors, Quantum Cellular automata, Light emitting diodes and lasers, Carbon nanotube transistors, Semiconductor nanowire FETs and SETs, Molecular SETs and Molecular Electronics.

UNIT V TUNNEL JUNCTIONS AND APPLICATIONS OF TUNNELING
Tunnelling through a potential barrier, Potential energy profiles in material interfaces, Applications of tunnelling, Field emissions, Gate oxide Tunnelling and Hot electron effects in MOSFETS, Scanning tunnelling microscope, Double barrier tunnelling and Resonant tunnelling diode

COURSE OUTCOMES:
CO1: Ability to familiarise the fundamental underpinnings of nano electronics.
CO2: Ability to analyse the electron properties of traditional low dimensional structures.
CO3: Analyse the growth, fabrication and measurement techniques of nanostructured devices.
CO4: Ability to analyse the key performance of nano electronic devices.
CO5: Ability to explore the basics of tunnelling devices.

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MEMS AND NEMS

UNIT I  INTRODUCTION AND FABRICATION OF MEMS
MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelorometers and Micro fluidics, Materials for MEMS: Silicon, silicon compounds, polymers, metals. Photolithography, Ion Implantation, Diffusion, Oxidation, Dry and wet etching, Bulk Micromachining, Surface Micromachining, LIGA

UNIT II  INTRODUCTION AND FABRICATION OF NEMS
Introduction to NEMS, Nano scaling, classification of nano structured materials, Applications of nanomaterials. Synthesis routes – Bottom up and Top down approaches. Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation

UNIT III  DESIGN OF MEMS SENSORS AND ACTUATORS
Acoustic sensor – Quartz crystal microbalance, Surface acoustic wave, Flexural plate wave, shear horizontal; Vibratory gyroscope, Pressure sensors, Electrostatic actuators, piezoelectric actuators, Thermal actuators, Actuators using shape memory alloys, Microgrippers, Micromotors, Microvalves, Micropumps.

UNIT IV  NEMS MATERIALS AND SENSORS
Quantum dots, Carbon nanotubes, Nanocrystalline ZnO, Nanocrystalline Titanium Oxide, Multilayered Films, Quantum well infrared photodetectors.

UNIT V  INTRODUCTION TO OPTICAL AND RF MEMS
Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF MEMS – design basics, case study – Capacitive RF MEMS switch, performance issues.

COURSE OUTCOMES:
At the end of the course student will be able to:
CO1: Recognize the basics of materials and fabrication of micro electromechanical systems.
CO2: Devise the fabrication techniques of nano electromechanical systems.
CO3: Analyze the key performance aspects of micro electromechanical sensors and transducers.
CO4: Analyze various aspects of nano materials and sensors.
CO5: Identify the potential applications of MEMS in the RF and optical domain.

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VL3052 FUNDAMENTALS OF SPINTRONICS AND QUANTUM COMPUTING  

UNIT I LAWS OF SPINTRONICS AND SPIN ORBIT  
The Early History of Spin, Quantum Mechanics of Spin, Spin – Orbit interaction, Spin – Orbit interaction of Solids.

UNIT II SPIN ELETRON TRANSPORT  
Basic Electron Transport, Basic Electron Transport in thin film, Conduction in Discontinuous film, Magneto-resistance, Spin-Dependent Scattering, Giant Magneto Resistance, Spin Dependent Tunneling, Tunnel Magnetoresistance, MTJ, STT, SOT.

UNIT III SPIN TRANSISTOR  
Silicon based spin electron device, Spin field effect transistor Spin injection, spin diffusion, Spin LED: Fundamental and Application, Spin photo electronics Devices

UNIT IV ELECTRON SPINS IN QUANTUM DOTS AS QUBITS  

UNIT V QUANTUM COMPUTING WITH SPINS  

TOTAL: 45 PERIODS

COURSE OUTCOMES:
At the end of this course students will be able to
CO1: Ability to learn the laws of spintronics and spin orbit.
CO2: Ability to obtain spin based transport and its characteristics.
CO3: Identify the types of spintronics based devices.
CO4: Design quantum gates using qubits.
CO5: Apply the quantum principles to quantum universal gates.

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AP3010  SYSTEM DESIGN USING HARDWARE DESCRIPTION LANGUAGES  L T P C  2 0 2 3

UNIT I  BASICS OF VHDL  6
Entity declaration - Architecture body - Creating I/O Ports for Different Data Types – Signal, Constant and variable - VHDL operators - Assignment operators, Logical operators, arithmetic operators and shift operators – Generic statement – VHDL statements - concurrent signal assignment statements and sequential statements – Packages, Components, Functions and Procedures – Test bench.

UNIT II  BASICS OF VERILOG  6

UNIT III  SYSTEM DESIGN WITH VHDL AND VERILOG  6

UNIT IV  DESIGN CONSIDERATIONS VERIFICATION  6
Timing Parameters – Metastability – Positive and Negative Clock skew – Setup slack and Hold slack – Clock latency – Area, Speed and Power requirements, Testing and verification.

UNIT V  CASE STUDIES  6
A Pipelined Multiplier Accumulator – ALU Design – Single port and Dual port Memory design – Design of ALU, DSP modules and MAC unit.

44
LAB EXPERIMENTS:
1. Implementation of Logic gates
2. Implementation of Mux and Demux
3. Implementation of Encode and Decoder
4. Implementation of Adders and Subtractors
5. Implementation of Flip-flops
6. Implementation of Counters
7. Implementation of registers
8. Implementation of simple state machine

TOTAL: 30+30 = 60 PERIODS

COURSE OUTCOMES:
At the end of this course students will be able to:
CO1: Understand the basic data types and operators of Verilog
CO2: Understand the basic data types and operators of VHDL
CO3: Design arithmetic modules using Verilog and VHDL
CO4: Analyse power dissipation and propagation delay of the RTL modules
CO5: Design macro modules such as ALU, MAC etc

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VL3055 NEUROMORPHIC COMPUTING L T P C 3 0 0 3

UNIT I INTRODUCTION TO NEUROMORPHIC ENGINEERING
Introduction to neuromorphic engineering, Non-von Neumann computing approach, Neuron, Synapse, Synaptic plasticity rules, spike-time-dependent plasticity, Signaling and operation of Biological neurons, Neuron models- LIF, IF, HH.

UNIT II SENSORY SYSTEMS AND LEARNING
Silicon retina, silicon cochlea, electronic nose, learning in silicon – supervised and unsupervised

UNIT III NEUROMORPHIC COMPUTING 9

UNIT IV NEUROMORPHIC HARDWARE IMPLEMENTATION 9

UNIT V NETWORK DESIGN 9
Network Design, Network design example for visual application, auditory application, full system level power/energy dissipation considerations.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to learn how electronics circuits mimic biological neurons.
CO2: Ability to implement learning techniques and cognitive functions in Silicon.
CO3: Ability to build power-saving hardware building blocks for neuromorphic systems.
CO4: Ability to design and develop neuromorphic circuits.
CO5: Ability to implement commercial neuromorphic system design for various real-world applications.

REFERENCES:

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UNIT I  INTRODUCTION TO MACHINE LEARNING ARCHITECTURE
Artificial Neural Networks – Artificial Neuron and its mathematical model, Activation functions, Biases and threshold, Linear separability, Neural network architecture: single layer and multilayer feed forward networks, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning, Architecture for Multiply and Accumulate unit, Special function unit for Sigmoid and ReLu activation functions.

UNIT II  SUPERVISED LEARNING AND UNSUPERVISED LEARNING

UNIT III  DEEP NEURAL NETWORKS
Convolutional Neural basics: kernels, padding, stride, channels, activation maps, Convolutional neural network: pooling, receptive field, batch normalization, Standard CNN architectures: LeNet, AlexNet, VGG, Inception, ResNet, GoogleNet, DenseNet; Performance comparison of different CNN architectures.

UNIT IV  VLSI IMPLEMENTATION OF NEURAL NETWORKS
Processing element model, PE row, PE array design, Processing element tile design, Direct, FFT-based, Winograd-based, Matrix multiplication based convolutional strategies, architectures for low-energy support vector machines.

UNIT V  VLSI ARCHITECTURE FOR DEEP NEURAL NETWORKS
VLSI architecture for deep neutral networks, data and instruction flow in 2D systolic array architecture, Processing optimization in 2D systolic array, Pruning, compression, Hardware Accelerator.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
CO1: Ability to build hardware blocks for neurons model
CO2: Ability to implement machine learning techniques
CO3: Ability to analyze digital implementations of Neural Network
CO4: Ability to implement deep neural networks
CO5: Ability to design energy-efficient machine learning hardware for deep neural network models.

REFERENCES:
2. Ethem Alpaydin, Introduction to Machine Learning, PHI
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